# 3.6V-36V Vin, 3.5A, High Efficiency Synchronous Step-down DCDC Converter

AEC-Q100 Qualified with the Following Results:
- Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Device HBM ESD Classification Level H2
- Device CDM ESD Classification Level C3B

Wide Input Range: 3.6V-36V

Up to 3.5A Continuous Output Current

1V ±1% Feedback Reference Voltage

Integrated 60 -Side and 36 Low-Side Power MOSFETs

Pulse Skipping Mode (PSM) with 25uA Quiescent Current in Sleep Mode

60ns Minimum On-time

4ms Internal Soft-start Time

400kHz Switching Frequency

Frequency Spread Spectrum (FSS) Modulation for EMI Reduction

Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis

Parallel input path to minimize switch node ringing

Low Dropout Mode Operation

Over-voltage and Over-Temperature Protection

Available in 2mm*3mm QFN-12L Package

Automotive infotainment and ADAS

USB Type-C Power Delivery, USB Charging

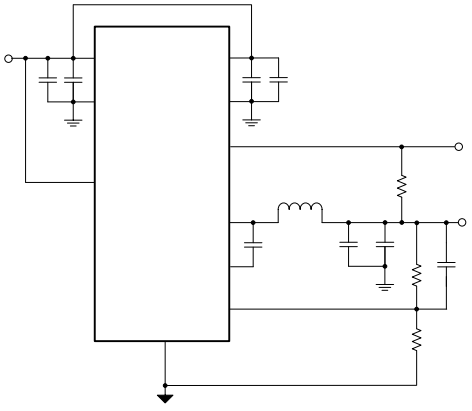
Industrial and Medical Distributed Power Supplies

The SCT2434AQ is 3.5A synchronous buck converters with wide input voltage, ranging from 3.6V to 36V, which integrates a 60 high-side MOSFET and a 36 -side MOSFET. The SCT2434AQ, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 25uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

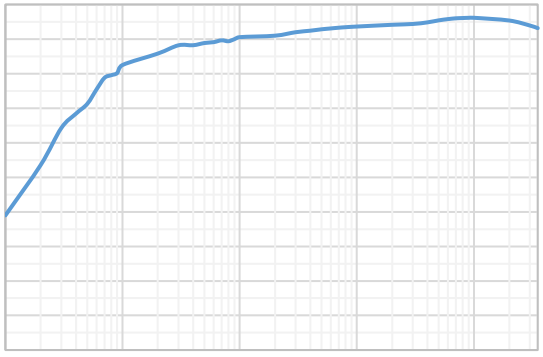
The SCT2434AQ features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency is fixed 400kHz. The SCT2434AQ allows power conversion from high input voltage to low output voltage with a minimum 60ns on-time of high-side MOSFET.

The SCT2434AQ is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2434AQ features Frequency Spread Spectrum FSS with ±6% jittering span of the 400kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2434AQ offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in 2mm*3mm QFN-12L package with wettable flanks.



**3.6V-36V, Syncronous Buck Converter**



**Efficiency, $V_{OUT}$=5V, $F_{SW}$=400KHz**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Release to production.
Revision 1.1: Update Pin Functions.
Revision 1.2: Update the selection of resistor $R_4$ in APPLICATION INFORMATION.
Revision 1.3: Update $I_{LIM\_HS}$, PACKAGE INFORMATION and TAPE AND REEL INFORMATION.
Revision 1.4: Update DEVICE ORDER INFORMATION.
Revision 1.5: Update the limit of $I_{LIM\_HS}$ and $I_{LIM\_LSSRC}$.
Revision 1.6: Update THERMAL INFORMATION.

| ORDERABLE DEVICE | PACKAGING TYPE | STANDARD PACK QTY | PACKAGE MARKING | PINS | PACKAGE DESCRIPTION | MSL |
|---|---|---|---|---|---|---|
| SCT2434AQFPAR | Tape & Reel | 5000 | 434AQ | 12 | FCQFN2x3-12L | 1 |

Over operating free-air temperature unless otherwise noted(1)

| DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|
| VIN | -0.3 | 42 | V |
| EN | -0.3 | 42 | V |
| BOOT | -0.3 | 48 | V |
| SW | -1 | 42 | V |
| BOOT-SW | -0.3 | 6 | V |
| PG | -0.3 | 24 | V |
| FB | -0.3 | 6 | V |
| Operating junction temperature TJ(3) | -40 | 150 | °C |
| Storage temperature TSTG | -65 | 150 | °C |

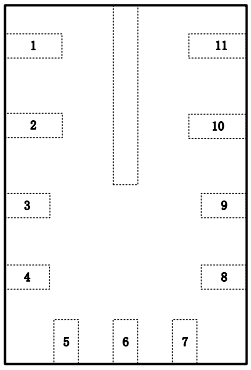



**Figure 1. 12-Lead QFN 2mm×3mm**

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

| NAME | NO. | PIN FUNCTION |
|---|---|---|
| PGND | 1,11 | Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection should be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1. |
| VIN | 2,10 | Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2. |
| NC | 3 | On the VQFN package, connect the SW pin to NC on the PCB. This simplifies the connection from the BOOT capacitor to the SW pin. This pin has no internal connection to the regulator. |

| | | |
|---|---|---|
| BOOT | 4 | High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and BOOT. An internal diode connects to VCC and allows BOOT to charge while SW node is low. |
| NC | 5 | This pin has no internal connection to the regulator. |
| AGND | 6 | Analog ground for internal circuitry. Feedback are measured with respect to this pin. Must connect AGND to both PGND1 and PGND2 on PCB. |
| FB | 7 | Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage. Do not float or connect to ground. |
| PG | 8 | Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PG output goes low when EN =low, VIN > 1V. |
| EN | 9 | Enable pin to regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold. |
| SW | 12 | Switching node of the buck converter. |

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 3.6 | 36 | V |
| $V_{OUT}$ | Output voltage range | 1 | 16 | V |
| $T_J$ | Operating junction temperature | -40 | 150 | °C |

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM) | -2 | +2 | kV |
| | Charged Device Model(CDM) | -1 | +1 | kV |

| PARAMETER | THERMAL METRIC | FCQFN2x3-12L | UNIT |
|---|---|---|---|
| $R_{}$ (1)(2) | Junction to ambient thermal resistance | 63.02 | °C/W |
| $_{JT}$ (2) | Junction-to-top characterization parameter | 3.33 | |
| $_{JB}$ (2) | Junction-to-board characterization parameter | 7.74 | |
| $R_{top}$ (1)(2) | Junction to case thermal resistance | 63.93 | |
| $R_{B}$ (2) | Junction-to-board thermal resistance | 7.95 | |
| $R_{\_EVM}$ (3) | Junction to ambient thermal resistance (EVM) | 52.9 | |
| $_{JT\_EVM}$ (3) | Junction-to-top characterization parameter (EVM) | 1.64 | |

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2434AQ is mounted and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT2434AQ. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

(3) Measured on SCT standard EVM: SCT2434AQ Demo Board, 1oz copper thickness, 75mm x 65mm, 4-layer PCB.

$V_{IN}$=24V, $T_J$=-40°C~125°C, typical value is tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 3.6 | | 36 | V |
| $V_{IN\_UVLO}$ | Input UVLO Threshold | $V_{IN}$ rising | | 3.4 | 3.6 | V |
| | Hysteresis | | | 300 | | mV |
| $I_{SHDN}$ | Shutdown current from VIN pin | EN=0 | | 1.2 | 10 | A |
| $I_Q$ | Quiescent current from VIN pin | EN floating, non-switching, BOOT-SW=5V | | 25 | 48 | A |
| **Power MOSFETs** | | | | | | |
| $R_{DSON\_H}$ | High-side MOSFET on-resistance | $V_{BOOT}$-$V_{SW}$=4.2V | | 60 | 100 | |
| $R_{DSON\_L}$ | Low-side MOSFET on-resistance | | | 36 | 65 | |
| **Reference** | | | | | | |
| $V_{REF}$ | Reference voltage of FB | $T_J$=25°C | 0.99 | 1 | 1.01 | V |
| | | $T_J$=-40°C~125°C | 0.985 | | 1.015 | V |
| **Current Limit and Over Current Protection** | | | | | | |
| $I_{LIM\_HS}$ | High-side power MOSFET peak current limit threshold | $T_J$=25°C | 4.3 | 5 | 5.7 | A |
| | | $T_J$=-40°C~125°C | 4.05 | | 6 | A |
| $I_{LIM\_LSSRC}$ | Low-side power MOSFET souring current limit threshold | $T_J$=25°C | 3.85 | 4.5 | 5.15 | A |
| | | $T_J$=-40°C~125°C | 3.525 | | 5.4 | A |
| **Enable and Soft Startup** | | | | | | |
| $V_{EN\_H}$ | Enable high threshold | | 1.17 | 1.24 | 1.31 | V |
| $V_{EN\_L}$ | Enable low threshold | | 1.05 | 1.12 | 1.19 | V |
| $I_{EN\_L}$ | Enable pin pull-up current | EN=1V | | 1 | | |
| $I_{EN\_H}$ | Enable pin pull-up current | EN=1.5V | | 4.8 | | uA |
| $T_{ss}$ | Internal soft start time | | | 4 | | ms |
| **Switching Frequency and External Clock Synchronization** | | | | | | |
| $F_{SW}$ | Switching frequency | $T_J$=25°C | 360 | 400 | 440 | kHz |
| | | $T_J$=-40°C~125°C | 320 | | 480 | kHz |
| $F_{JITTER}$ | Frequency spread spectrum in percentage of Fsw | | | ±6 | | % |
| $t_{ON\_MIN}$ | Minimum on-time | $V_{IN}$=36V | | 60 | | ns |
| **Power Good** | | | | | | |
| $V_{PG\_UV}$ | Power-good flag under voltage tripping threshold | POWER GOOD (% of FB voltage) | | 95 | | % |
| | | POWER BAD (% of FB voltage) | | 90 | | % |
| $V_{PG\_OV}$ | Power-good flag over voltage tripping threshold | POWER BAD (% of FB voltage) | | 110 | | % |
| | | POWER GOOD (% of FB voltage) | | 105 | | % |
| $I_{PG}$ | PWRGD leakage current at high level output | VPull-Up = 5V | | | 200 | nA |
| $V_{PG\_LOW}$ | PWRGD low level output voltage | IPull-Up = 1 mA | | 50 | | mV |
| $t_{PGDFLT(rise)}$ | Delay time to PGOOD high signal | | | 2 | | ms |

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PGDFLT(fall)}$ | Glitch filter time constant for PGOOD function | | | 130 | | us |
| **Protection** | | | | | | |
| $V_{OVP}$ | Feedback overvoltage with respect to reference voltage | $V_{FB}/V_{REF}$ rising | | 110 | | % |
| | | $V_{FB}/V_{REF}$ falling | | 105 | | % |
| $V_{BOOTUV}$ | | BOOT-SW falling | | 2.7 | | V |
| | | Hysteresis | | 400 | | mV |
| $T_{SD}$ | Thermal shutdown threshold* | $T_J$ rising | | 160 | | °C |
| | | Hysteresis | | 20 | | °C |

*Derived from bench characterization

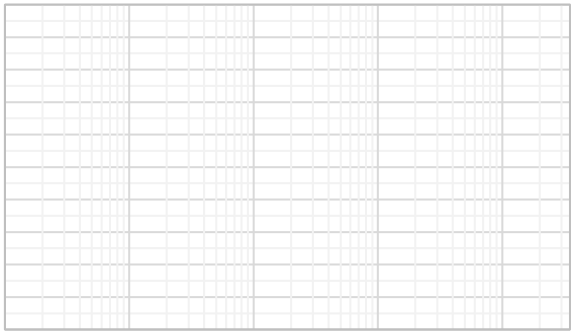


Figure 2. Efficiency, $F_{SW}$=400KHz, $V_{OUT}$=3.3V

Figure 3. Efficiency, $F_{SW}$=400KHz, $V_{OUT}$=5V

Figure 4. Line Regulation ($V_{OUT}$=5V, $I_{LOAD}$=3.5A)

Figure 5. Input Current ($V_{OUT}$=5V, $I_{LOAD}$=0A)

Figure 6. Load Regulation ($V_{OUT}$=5V)

Figure 7. Current Limit vs Temperature

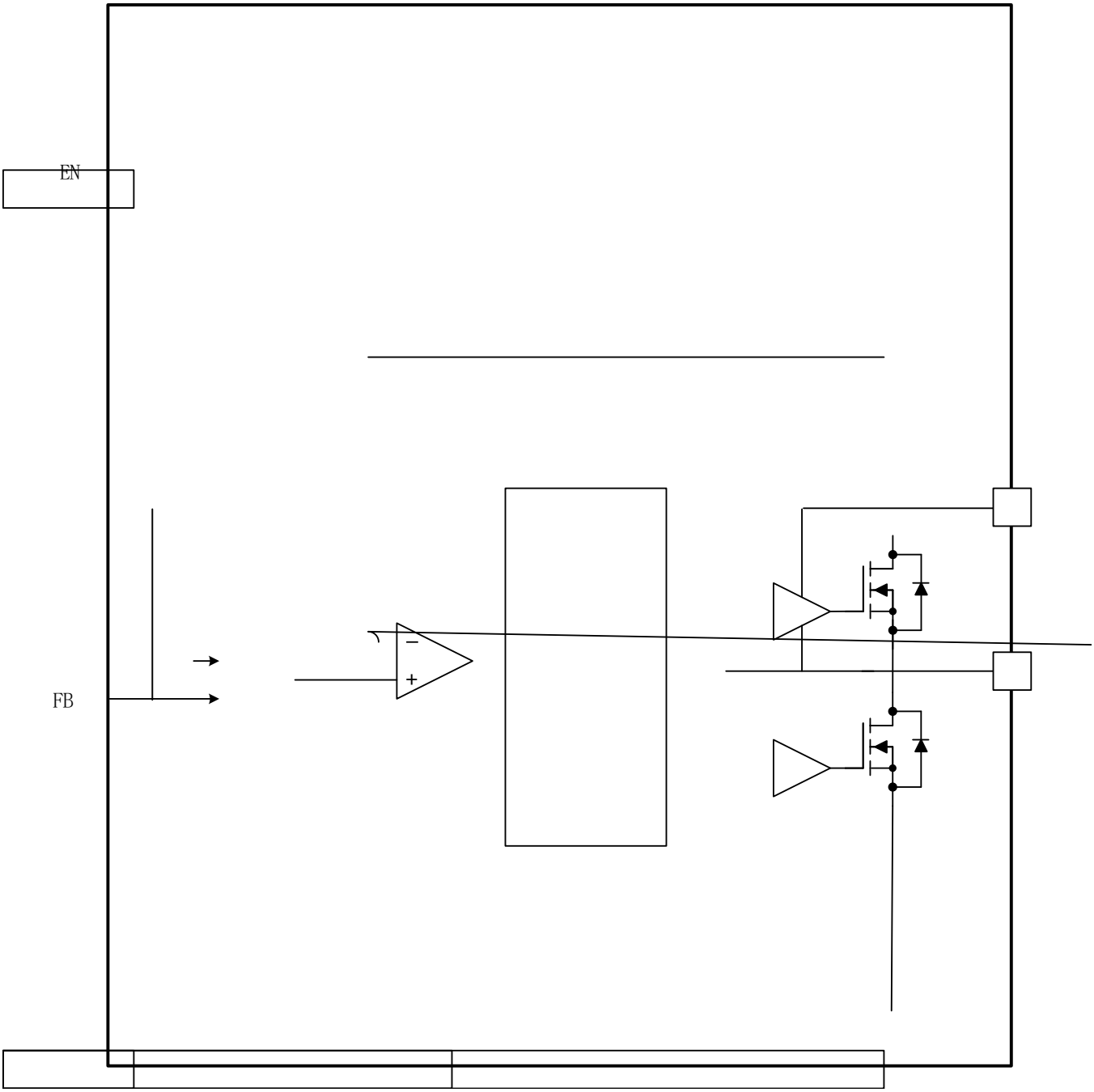



Figure 8. Functional Block Diagram

### Overview

The SCT2434AQ is a 3.6V-36V input, 3.5A output, EMI friendly synchronous buck converter with built-in 60m Rdson high-side and 36m Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is fixed 400kHz. The SCT2434AQ features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 25uA under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2434AQ implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2434AQ full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

### Peak Current Mode Control

The SCT2434AQ employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 1.0V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2434AQ operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 0.8A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 25uA during skipping period with no switching to improve efficiency further.

### Enable and Under Voltage Lockout Threshold

The SCT2434AQ is enabled when the VIN pin voltage rises about 3.4V and the EN pin voltage exceeds the enable threshold of 1.24V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.12V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

(1)

(2)

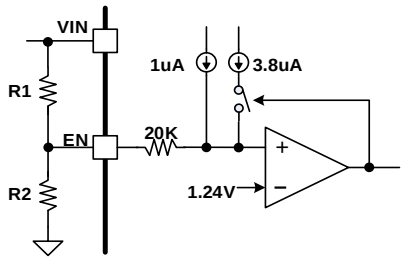



Figure 9. System UVLO by enable divide

where

$V_{rise}$ is rising threshold of Vin UVLO

$V_{fall}$ is falling threshold of Vin UVLO

$I_1$=1uA, $I_2$=3.8uA, $V_{ENR}$=1.24V, $V_{ENF}$=1.12V

### Output Voltage

The SCT2434AQ regulates the internal reference voltage at 1.0V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

(3)

where

$R_{FB\_TOP}$ is the resistor connecting the output to the FB pin.

$R_{FB\_BOT}$ is the resistor connecting the FB pin to the ground.

### Internal Soft-Start

The SCT2434AQ integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.0V reference voltage in 4mS. If the EN pin is pulled below 1.12V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

### Frequency Spread Spectrum

To reduce EMI, the SCT2434AQ implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency.

### Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 3.1V and hysteresis of 400mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.7V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2434AQ operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 3.1V. When the voltage from BOOT to SW drops below 2.7V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 3.1V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2434AQ LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

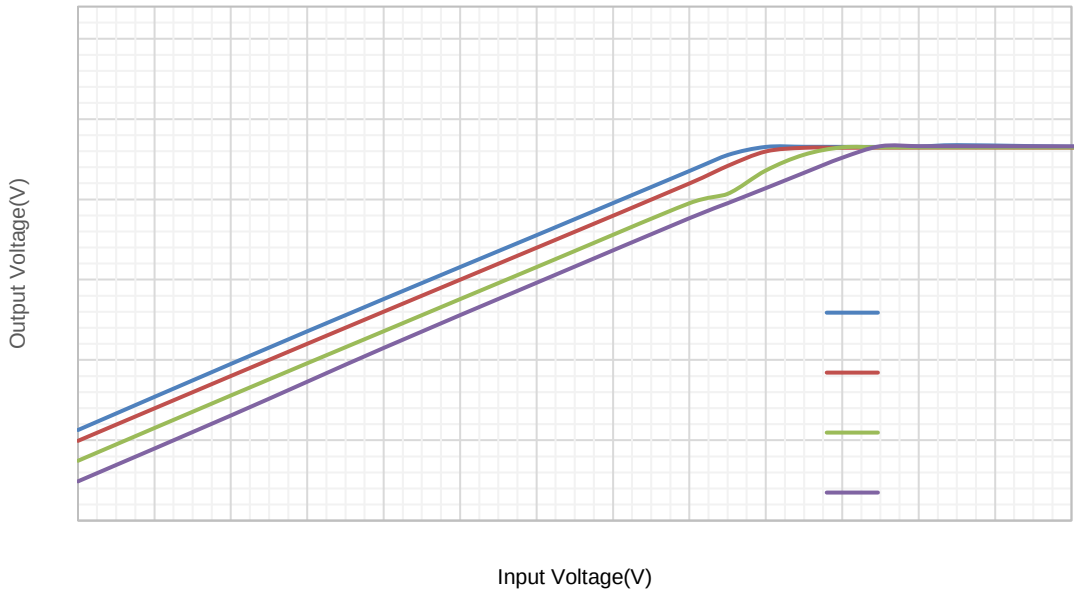



Figure 10. LDO Operation Characteristic ($V_{OUT}$=5V)

### Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2434AQ implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage 1.7V typical. When COMP voltage is clamped for 16 cycles of low side OC, the converter stops switching. After remaining OFF for 33.6ms，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high ， after soft start time and COMP still keep high for 16 cycles of low side OC，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

### Over voltage Protection

The SCT2434AQ implements the Over-Voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 1.0V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 1.0V reference voltage, the high-side MOSFET can turn on again.

### Power Good

The PG pin is an open-
that is 5V or less is recommended.

Once the FB pin is between 95% and 105% of the internal voltage reference the PG pin is de-asserted and the pin floats with 2ms delay. The PG pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage with 130us deglitching time. Also, the PG is pulled low if Vin UVLO or thermal shutdown are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 130us deglitching time do not trip the PG flag.

### Thermal Shutdown

The SCT2434AQ protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 160°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 140°C, the device restarts with internal soft start phase.

llr TJR e4ea20(y)-6(ea)1dTOq0.00000912 0 612 792 reW* nBT/F3 8.04 Tf1 0 0 1 69.624 4483Tmm0 G[ )-5( )9( 3(o)4(r)5(ma)16(t)-5(ion)6( )-5(inf)-3(o)4(r)5(ma)16(t)1 0 0 1

### Output Voltage

The output voltage is set by an external resistor divider $R_3$ and $R_4$ in typical application schematic. When the output voltage is greater than 3V, recommended $R_4$ resistance is 24.9K . Use equation 4 to calculate $R_3$.

(

| $V_{OUT}$ | $R_3$ | $R_4$ |
|---|---|---|
| 3.3 V | 57.6 | 24.9 |
| 5 V | 100 | 24.9 |
| 12 V | 274 | 24.9 K |

(4)

where:

$V_{REF}$ is the feedback reference voltage, typical 1V

If the output voltage is less than 3V, $R_4$ cannot exceed 24 .

### Under Voltage Lock-Out

An external voltage divider network of $R_1$ from the input to EN pin and $R_2$ from EN pin to the ground can set the -Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.9V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.1V (stop or disable). Use Equation 5 and Equation 6 to calculate the values 309 76.8 $_1$ and $R_2$ resistors.

(5)

(6)

where:

$V_{rise}$ is rising threshold of Vin UVLO

$V_{fall}$ is falling threshold of Vin UVLO

$I_1$=1uA, $I_2$=3.8uA, $V_{ENR}$=1.24V, $V_{ENF}$=1.12V

### Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor $I_{LPP}$ can be calculated as in Equation 7.

(7)

Where

$I_{LPP}$ is the inductor peak-to-peak current
L is the inductance of inductor

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 11.

(11)

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

(12)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

(13)

For this example, two 4.7 , X7R ceramic capacitors rated for 50 V in parallel are used. And a - frequency filtering capacitor is placed as close as possible to the device pins.

**Bootstrap Capacitor Selection**

A 0.1 r must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

**Output Capacitor Selection**

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

(14)

Where

enxUS



Wqcify(l)5(tag)-7(e )]TJETO EMC 2Span /MCID 196/Lang (en-US)>> BDC q0.00000912 0 612 792 reW* nBT/F3 9.962Tf1 20f174.904 233

**Table 2: Typical External Component Values**

| | | | | | |
|---|---|---|---|---|---|
| | 57.6 | | | | |


1

## Application Waveforms

$V_{IN}$=12V, $V_{OUT}$=5V, unless otherwise noted

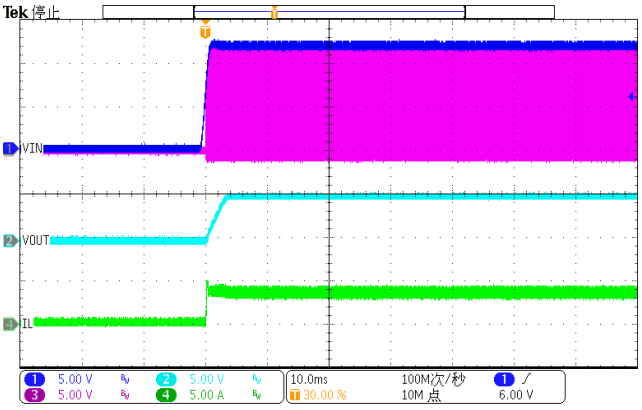



Figure 12. Power up($I_{LOAD}$=3.5A)

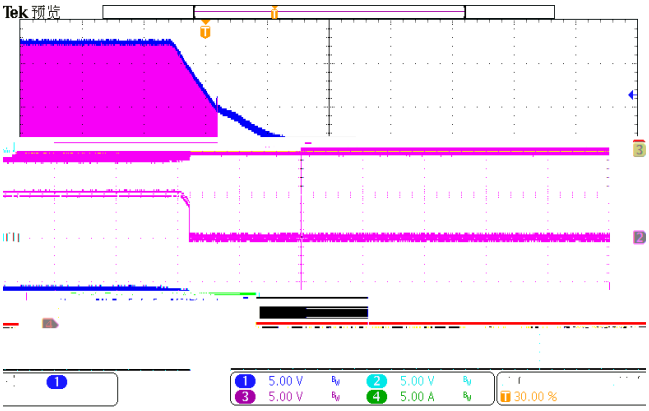



Figure 13. Power down($I_{LOAD}$=3.5A)

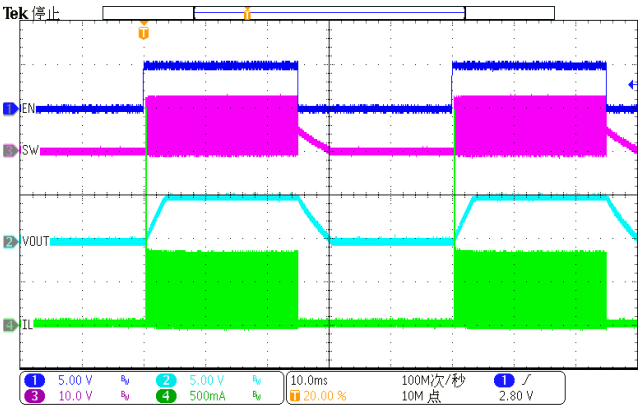



Figure 14. EN toggle ($I_{LOAD}$=0.1A)

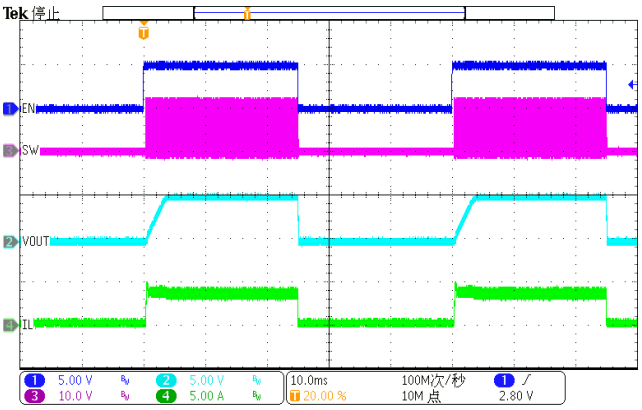



Figure 15. EN toggle ($I_{LOAD}$=3.5A)

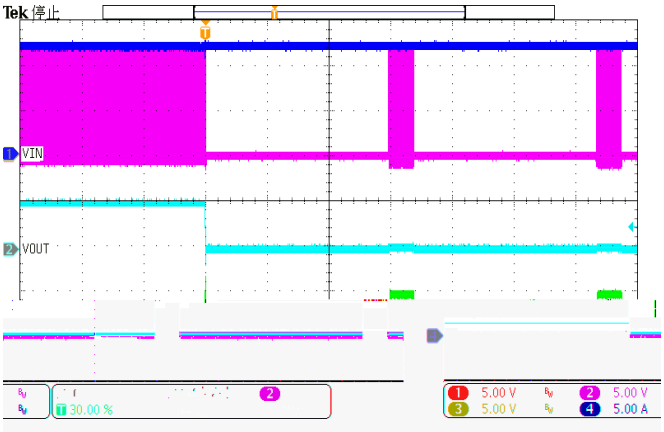



Figure 16. Over Current Protection(1A to hard short)

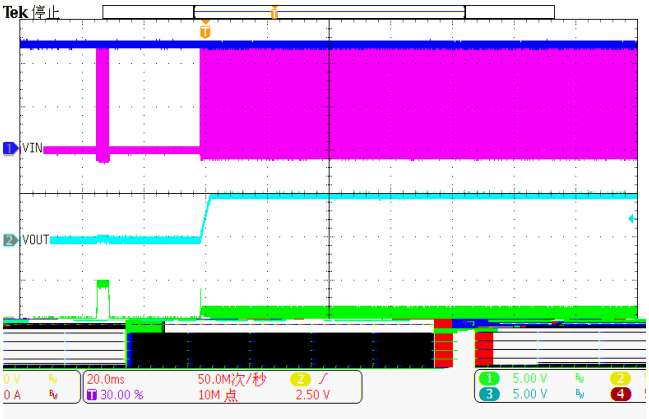



Figure 17. Over Current Release (hard short to 1A)

## Application Waveforms

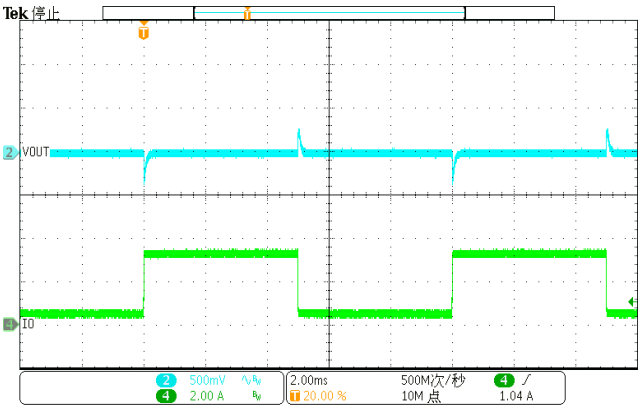



Figure 18. Load Transient (0.35A-3.15A, 1.6A/us)

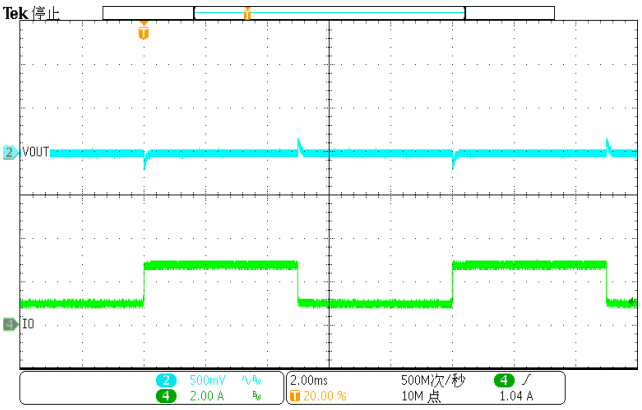



Figure 19. Load Transient (0.87A-2.63A, 1.6A/us)

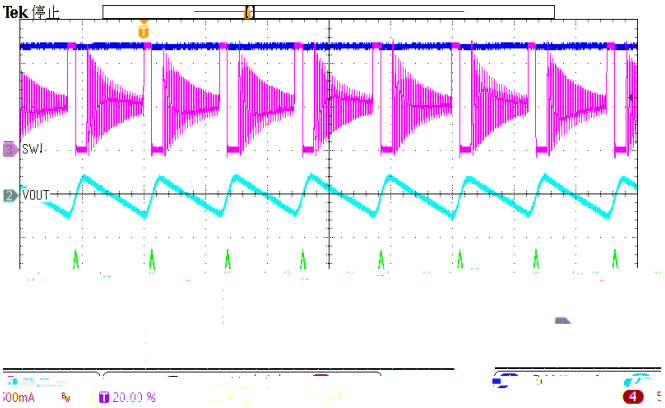



Figure 20. Output Ripple ($I_{LOAD}$=100mA)

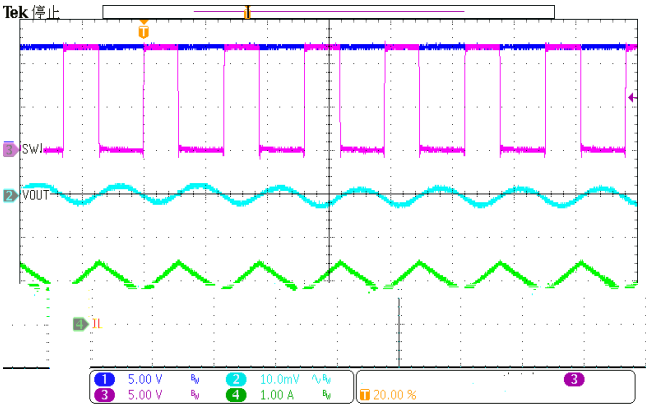



Figure 21. Output Ripple ($I_{LOAD}$=1A)

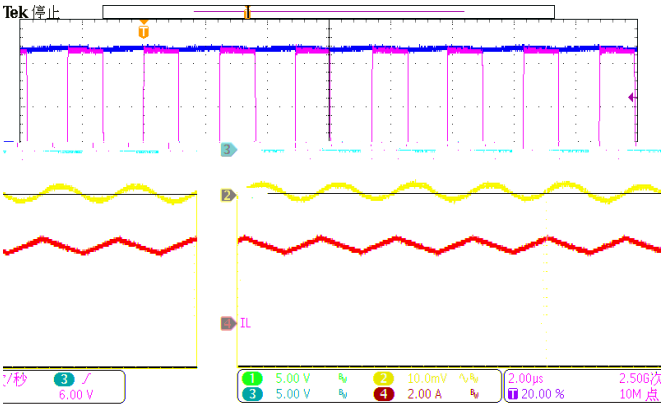



Figure 22. Output Ripple ($I_{LOAD}$=3.5A)

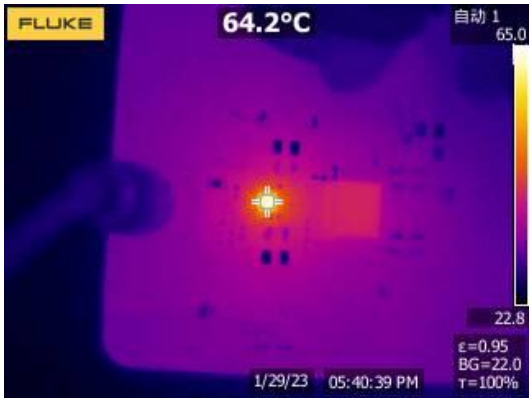



Figure 23. Thermal, 12$V_{IN}$, 5$V_{OUT}$, 3.5A

**Layout Guideline**

Proper PCB layout is a critical for SCT2434AQ . The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying po n0 yRQ