3.8V-32V Vin, 2A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 500kHz Switching Frequency
- Force Pulse Width Modulation (FPWM) Mode
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 130 R_{dson} High Side MOSFET and 70 R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

APPLICATIONS

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

DESCRIPTION

The SCT2321 is a 2A synchronous buck converter with up to 32V wide input voltage range, which fully integrates a 1

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.1 Released to Production. Complete orderable information.

Revision 1.2 Released to Production. Updated application waveforms.

Revision 1.3: Delete VS in ABS table.

Revision 1.4: Update Device Order Information.

Revision 1.5: Update PACKAGE INFORMATION.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2321TVBR	Tape & Reel	3000	2321	6	TSOT23-6L

ABSOLUTE MAXIMUM RATINGS

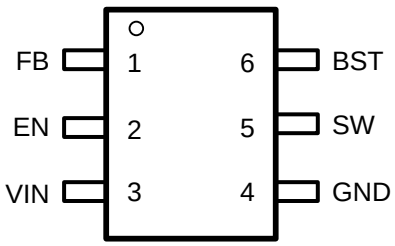
Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
FB	-0.3	5.5	V
Operating junction temperature(2)	-40	125	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN CONFIGURATION



Top View: TSOT23-6L, Plastic

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
FB	1	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1,1V falling for programmable UVLO threshold and hysteresis.
VIN	3	Power supply input. Must be locally bypassed.
GND	4	Power ground. Must be soldered directly to ground plane.
SW	5	Switching node of the buck converter.

BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	32	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6L	UNIT
R	Junction to ambient thermal resistance(1)	89	°C/W
R	Junction to case thermal resistance(1)	39	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2321 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2321. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		32	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.5 	3.7 	V

TYPICAL CHARACTERISTICS

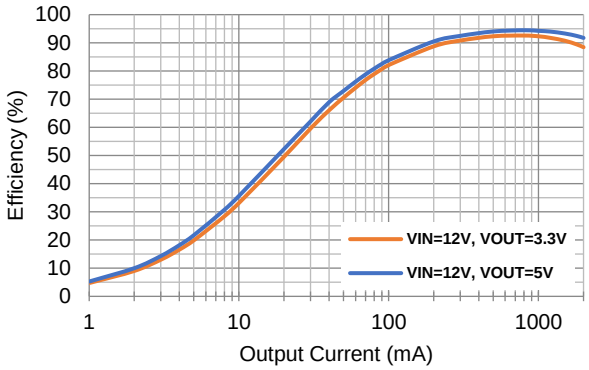


Figure 1. SCT2321 Efficiency, Vin=12V

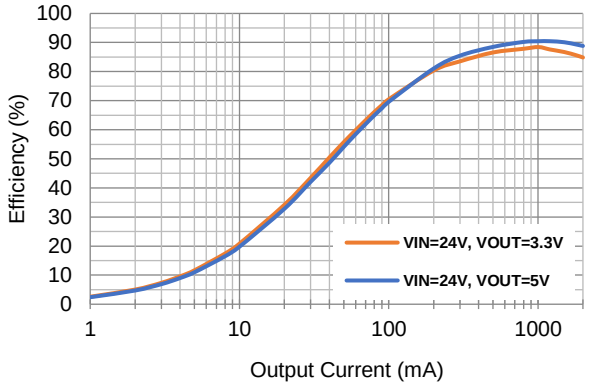


Figure 2. SCT2321 Efficiency, Vin=24V

Figure 3. Shut-down Current vs Temperature

Figure 4. Reference Voltage vs Temperature

Figure 5. Peak Current Limit vs Temperature

Figure 6. VIN UVLO vs Temperature

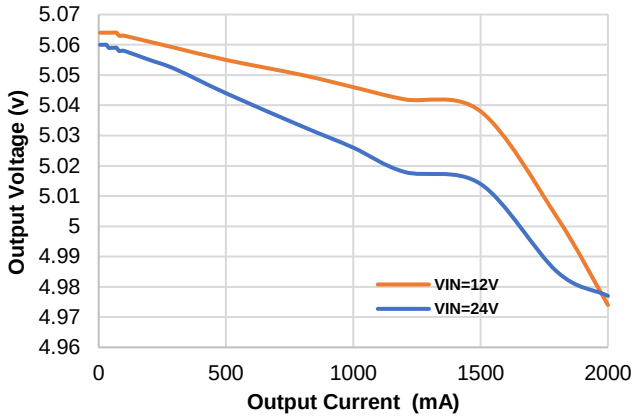


Figure 7. Load Regulation, (VOUT=5V)

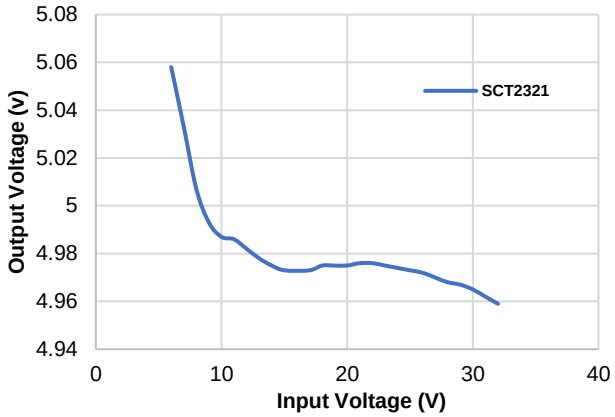
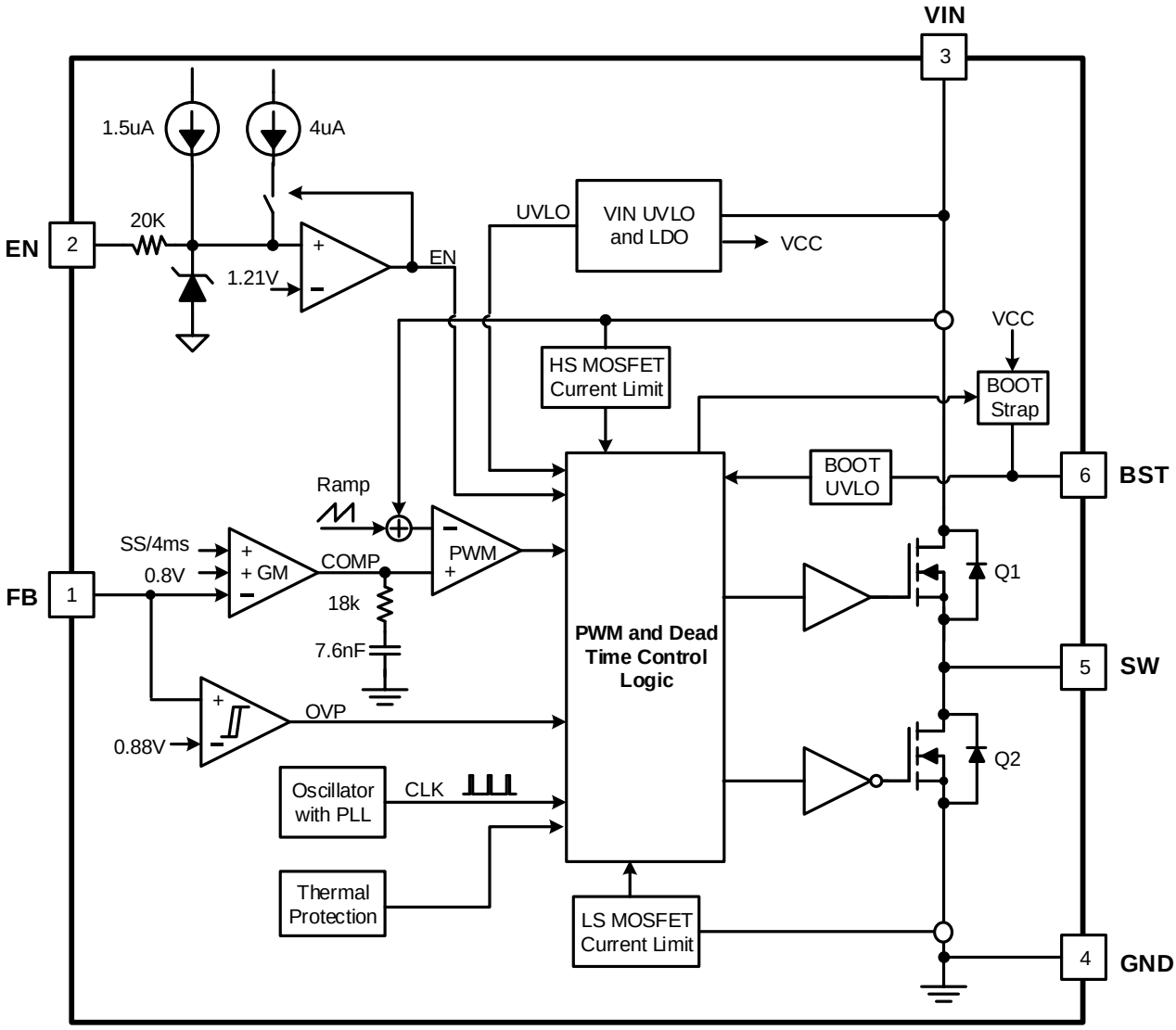


Figure 8. Line Regulation (IOUT=2A)

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT2321 device are 3.8V-32V input, 2A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 500kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT2321 footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2321 converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

To provide the lower output ripple in light load condition, the SCT2321 offers the fixed 500kHz switching frequency and works at the Force Pulse Width Modulation (FPWM) mode.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT2321 device also feature full protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2321 is designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2321 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT2321 enable all functions and the device starts soft-start phase. The SCT2321 have the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating

EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 9. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin, and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

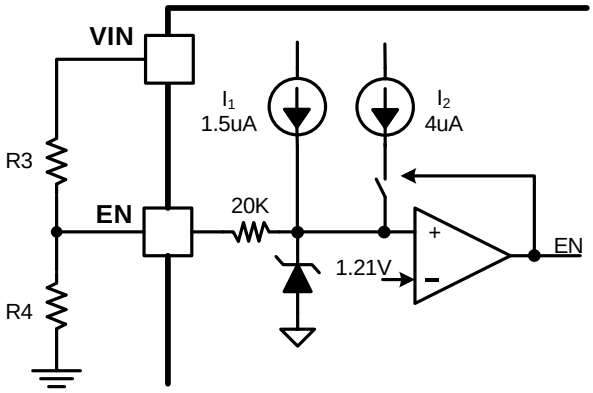


Figure 9. Adjustable VIN UVLO

(1)

(2)

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=4uA
V_{ENR}=1.18V
V_{EMF}=1.1V

EMI Reduction with Switching Node Ringing-free

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2321 implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 10.

Figure 10. SCT2321 Switching Node Waveform

Peak Current Limit and Hiccup Mode

The SCT2321 hav

Thermal Shutdown

Once the junction temperature in the SCT2321 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

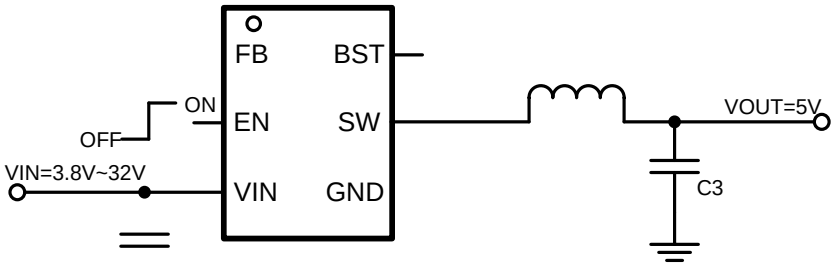


Figure 11. 24V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	500kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 recommended for the decoupling capacitor anda0.1 to be placed as close as possible to the VIN pin of the SCT2321.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of avior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

(5)

Set the current limit of the SCT2321 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2321. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744314101 is used on SCT2321 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744314101	10	33	3.5	7x7x5	Wurth Electronik

Output Capacitor Selection

For b

- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor

Application Waveforms

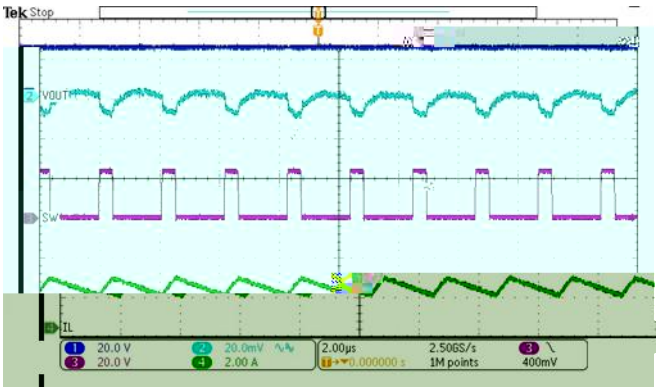


Figure 12. SW node waveform and Output Ripple
VIN=24V, IOUT=2A

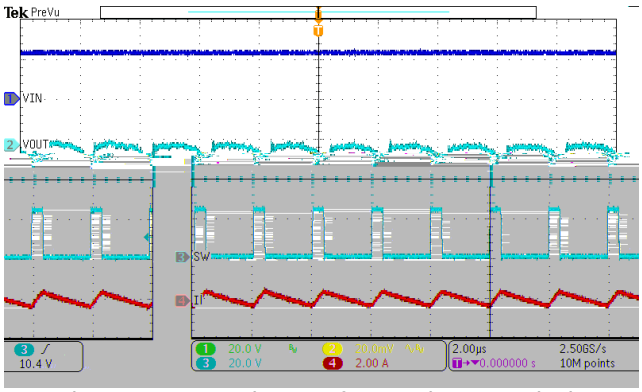


Figure 13. SW node Waveform and Output Ripple
VIN=24V, IOUT=10mA

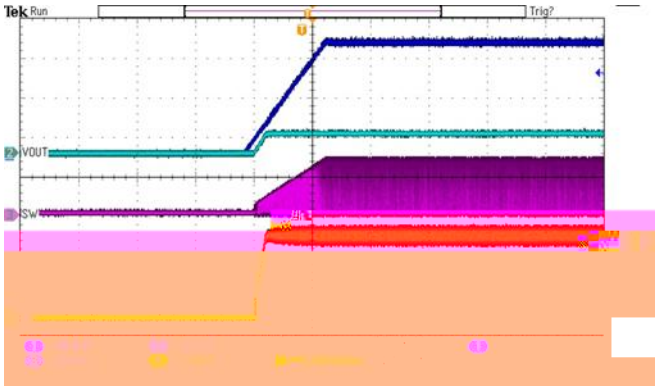


Figure 14. Power Up
VIN=24V, VOUT=5V, IOUT=2A

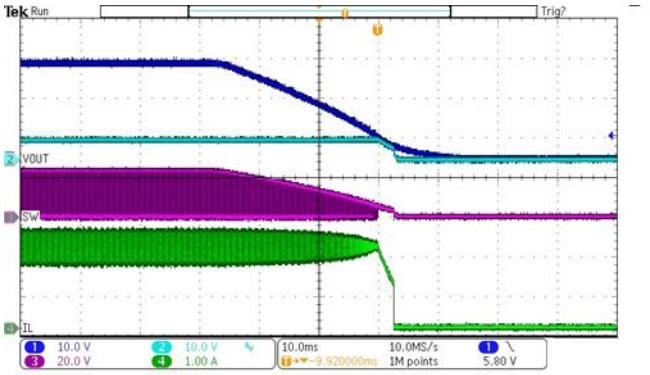


Figure 15. Power Down
VIN=24V, VOUT=5V, IOUT=2A

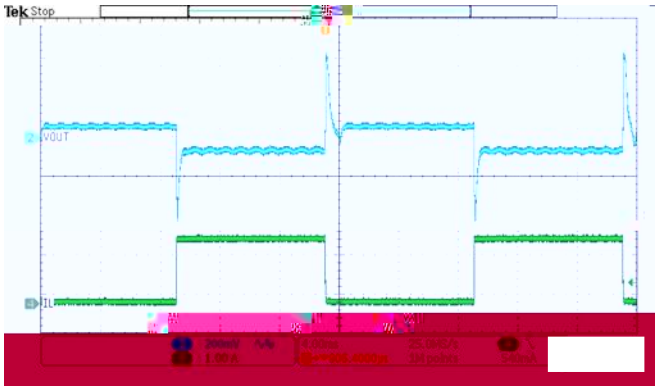


Figure 16. Load Transient
VOUT=5V, IOUT=0.2A to 1.8A, SR=250mA/us

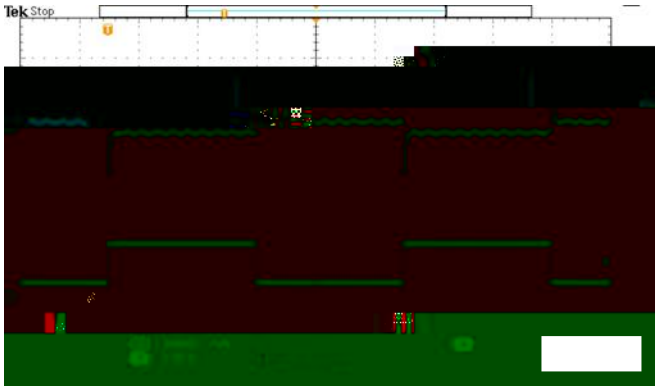


Figure 17. Load Transient
VOUT=5V, IOUT=0.5A to 1.5A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 18 is the recommended PCB layout of SCT2321.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

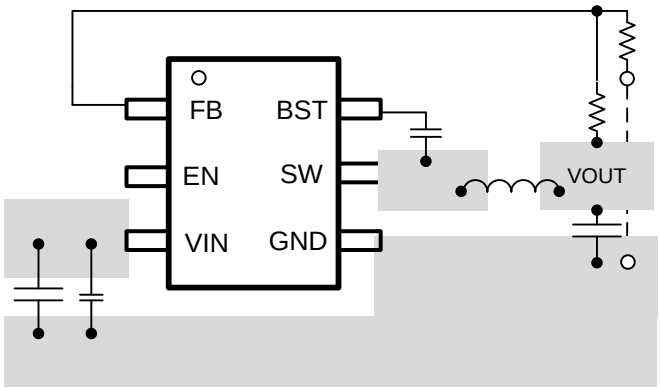


Figure 18. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

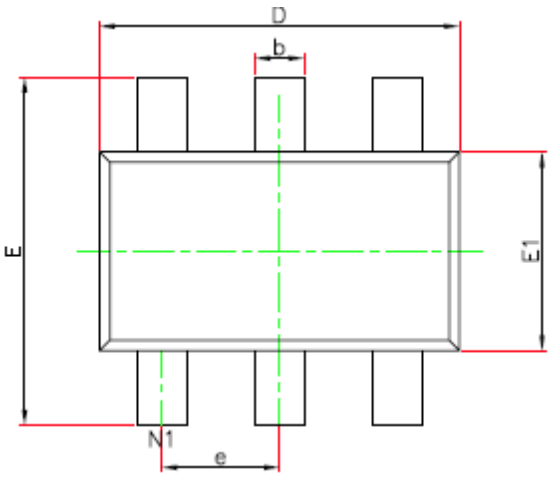
(12)

where

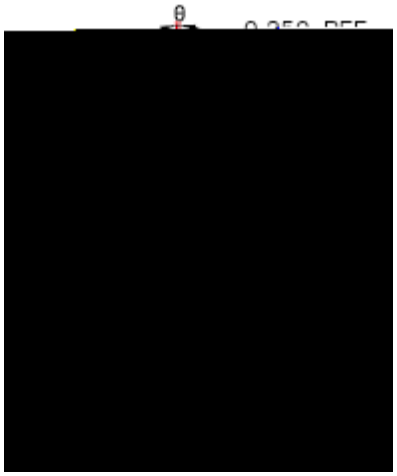
- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

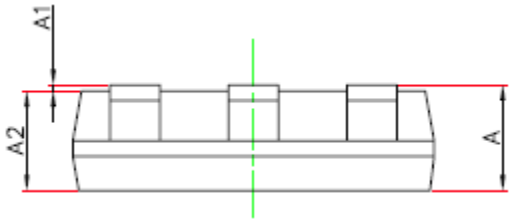
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-------		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
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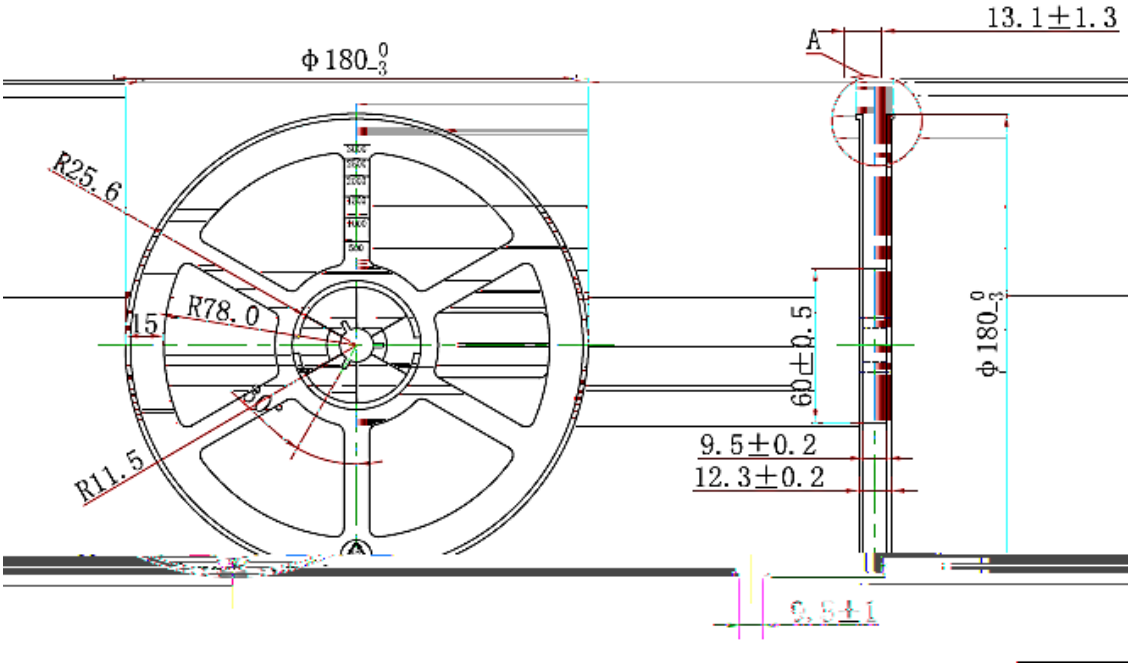
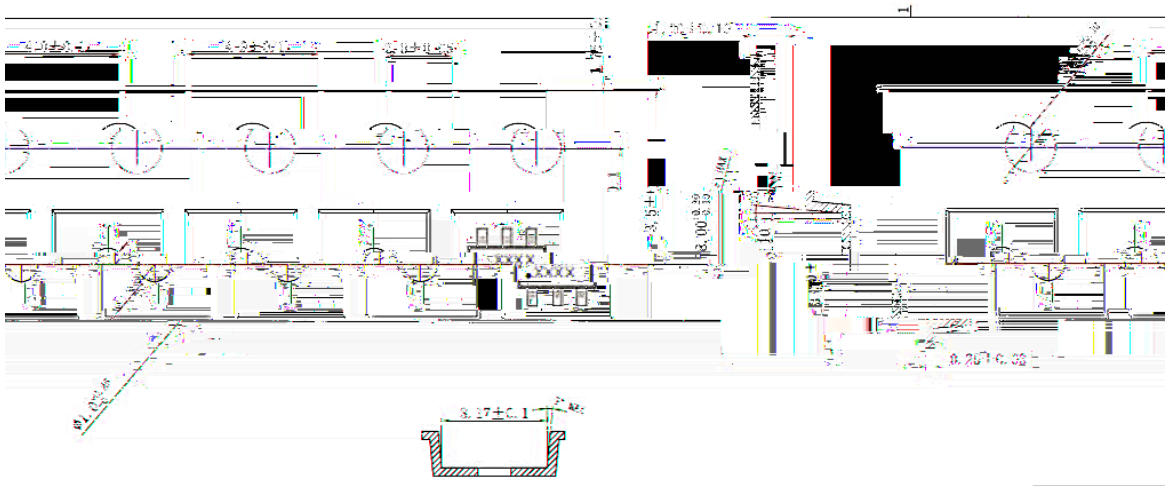
TAPE AND REEL INFORMATION





Feeding Direction

RELATED PARTS

PN	DESCRIPTION	COMMENTS
SCT2325 **SCT2323**	3.8V-32V Vin, Fixed Vout, 2A Synchronous Buck Converter with EMI Reduction	• 1.1MHz switching frequency with ±6% FSS • EMI reduction with switching node ringing-free. • SW anti-ringing in discontinuous current mode • 20uA ultra-low quiescent current • Minimum external components. Easy-to-use • Fixed 5V Vout (SCT2325) and 3.3V Vout (SCT2323)
SCT2330 **SCT2331**	3.8V-32V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction	• 500KHz switching frequency • 3A Continuous output current • EMI reduction with switching node ringing-free. • Ultra-low quiescent current. High efficiency PFM at

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