4.5V-60V Vin, 1A, High Efficiency Step-down DCDC Converter

Qualified for Automotive Applications
AEC-Q100 Qualified with the Following Results:
- Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
Wide Input Range: 4.5V-60V
Continuous Output Current: 1A
0.765V Feedback Reference Voltage
Integrated 500mΩ High-Side
Low Quiescent Current: 80uA
Pulse Skipping Mode (PSM) in light load
80ns Minimum On-time
6ms Internal Soft-start Time
Internal compensation
Switching Frequency 480KHz
Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
Low Dropout Mode Operation
Over-voltage and Over-Temperature Protection
Available in an TSOT23-6L Package

12-V, 24-V, 48-V Industry and Telecom Power System
Industrial Automation and Motor Control
Vehicle Accessories

The SCT2613Q is 1A buck converter with wide input voltage, ranging from 4.5V to 60V, which integrates an 500mΩ high-side MOSFET. The SCT2613Q, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with 80uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2613Q features fixed 480KHz switching frequency, which minimizes the external off chip passive components size and reduces the output ripple. The SCT2613Q allows power conversion from high input voltage to low output voltage with a ming it

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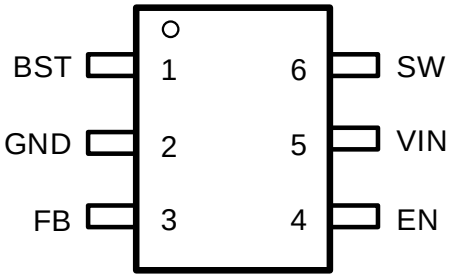
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Release to production.

SCT2613QTVBR	Tape & Reel	3000	2613Q	6	TSOT23-6L	3

Over operating free-air temperature unless otherwise noted [1]

VIN, EN [2]	-0.3	65	V
BST	-0.3	72	V
SW	-1	65	V
SW (<20ns) [3]	-5	65	V
BST-SW	-0.6	6	V
FB	-0.3	6	V
Operating junction temperature TJ [4]	-40	150	°C
Storage temperature TSTG	-65	150	°C



(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

BST	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BST pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
GND		

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Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	60	V
V_{OUT}	Output voltage range	0.765	57	V
T_A	Operating ambient temperature	-40	125	°C

V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	- 1.5	1.5	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	- 1	1	kV

$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	134.25	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	22.68	
Ψ_{JB} (2)	Junction-to-board characterization parameter	43.34	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	81.31	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	44.09	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2613Q is mounted and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT2613Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		4.5		60	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising Hysteresis	4 100	4.23 200	4.45 600	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1.65	5	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching		80	150	μA
R_{DSON_H}	High-side MOSFET on-resistance			500	800	mΩ
V_{REF}	Reference voltage of FB		0.746	0.765	0.784	V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		1.5	2	2.4	A
V_{EN_H}	Enable high threshold		1.1			

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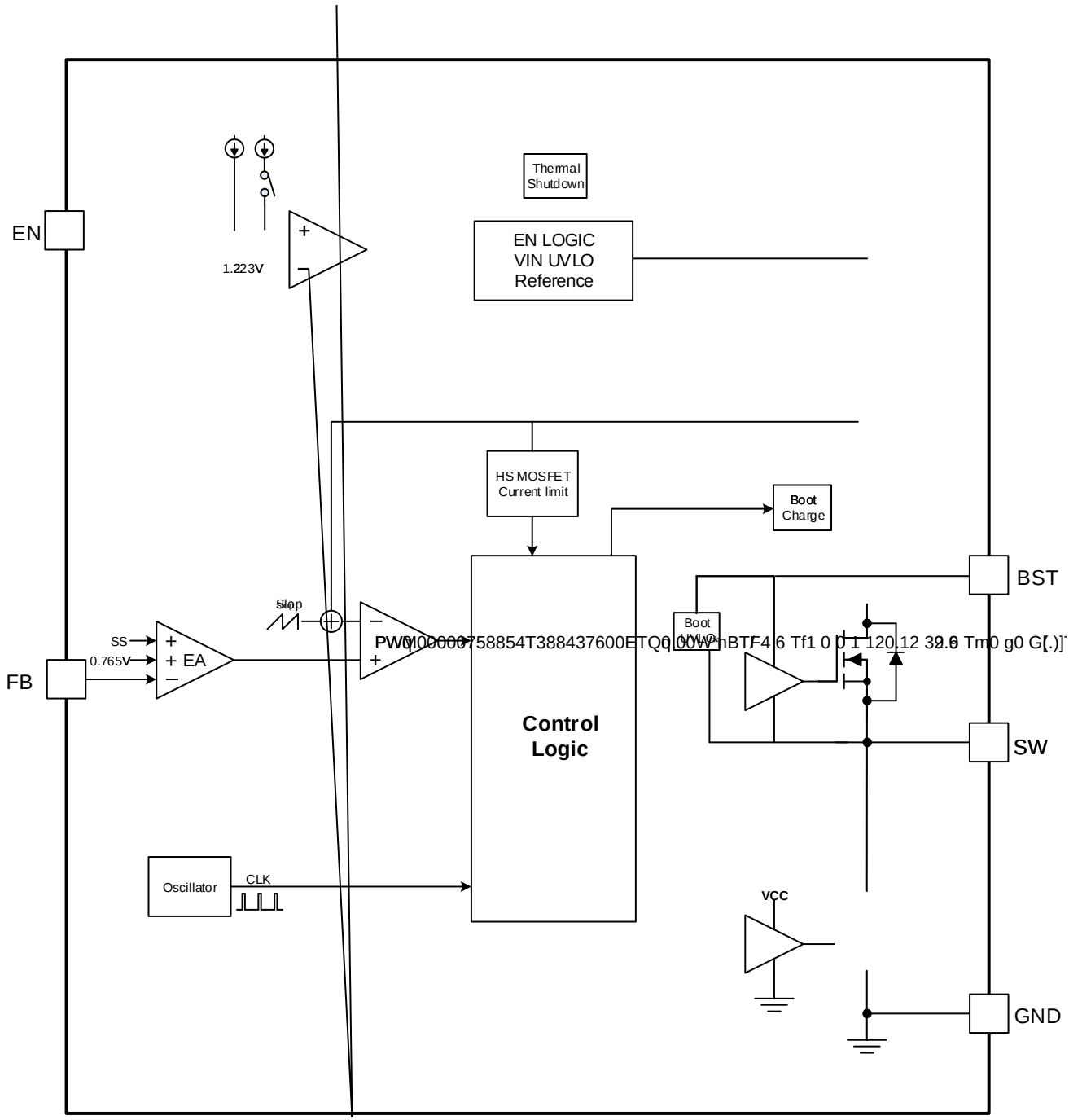

Figure 8. Functional Block Diagram

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The SCT2613Q is a 4.5V-60V input, 1A output, buck converter with integrated 500mΩ Rdson high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response.

The SCT2613Q features fixed 480KHz switching frequency, which minimizes the external off chip passive components size and reduces the output ripple. The SCT2613Q features an internal 6ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 80uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2613Q has a default input start-up voltage of 4.23V with 200mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2613Q full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

The SCT2613Q employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.765V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2613Q operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (470mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 160mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 80uA during skipping period with no switching to improve efficiency further.

The SCT2613Q is enabled when the VIN pin voltage rises above 4.23V and the EN pin voltage exceeds the enable threshold of 1.223V. The device is disabled when the VIN pin voltage falls below 4.03V or when the EN pin voltage is below 1.13V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

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power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2613Q LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

The SCT2613Q implements over current protection with fold back current limit. The SCT2613Q cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously.

The SCT2613Q implements frequency fold back to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.765 V to 0 V. The SCT2613Q uses a digital frequency fold back to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency fold back effectively increases the off-time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency fold back ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency fold back protection. Equation 4 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT}. The selected operating frequency must t

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The SCT2613Q protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 173°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 163°C, the device restarts with internal soft start phase.

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The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 5 to calculate R1.

$$_1 = (\frac{}{} - 1) \quad _2 \qquad (5)$$

where:

V_{REF} is the feedback reference voltage, typical 0.765V

OR	C bR R R ab R	ba baC a TR
3.3V	34.0 KΩ	10.2 KΩ
5V	56.2 KΩ	10.2 KΩ
12 V	147 KΩ	10.2 KΩ

An external voltage divider network of R_3 from the input to EN pin and R_4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 8V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 7 V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 127 kΩ and 22.1 kΩ of R_3 and R_4 resistors.

$$_3 = \frac{0.924 -}{3.076} \qquad (6)$$

$$_4 = \frac{_3 \times 1.13}{- 1.13 + \quad _3 \quad 4} \qquad (7)$$

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

$$= \frac{(\quad - \quad)}{} \qquad (8)$$

Where:

I_{LPP} is the inductor peak-to-peak current
L is the inductance of inductor
f_{SW} is the switching frequency
V_{OUT} is the output voltage
V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$= \frac{}{(\quad)} \quad (1 - \frac{}{(\quad)}) \qquad (9)$$

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Where:

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I

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If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$= \frac{(\quad - \quad) \times \quad \times}{} + \frac{\times \quad \times (\quad + \quad)^2}{2} \tag{12}$$

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} \quad \sqrt{\frac{V_{OUT}}{V_{IN}} \quad (1 - \frac{V_{OUT}}{V_{IN}})} \tag{13}$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 \quad I_{OUT} \tag{14}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \quad C_{IN}} \quad \frac{V_{OUT}}{V_{IN}} \quad (1 - \frac{V_{OUT}}{V_{IN}}) \tag{15}$$

For this example, one 4.7μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1μF ceramic capacitor must be connected between BST pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

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$$\Delta V_{OUT} = \frac{(\quad - \quad)}{8 \quad {}^{2}} \tag{16}$$

Where:

ΔV_{OUT} is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

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Vin=24V, Vout=5V, unless otherwise noted

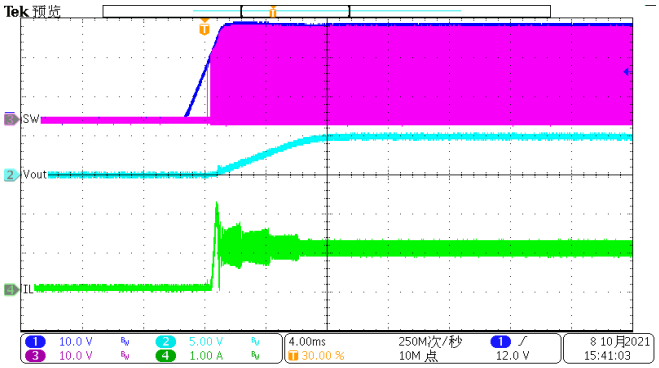

Figure 11. Power up(Iload=1A)

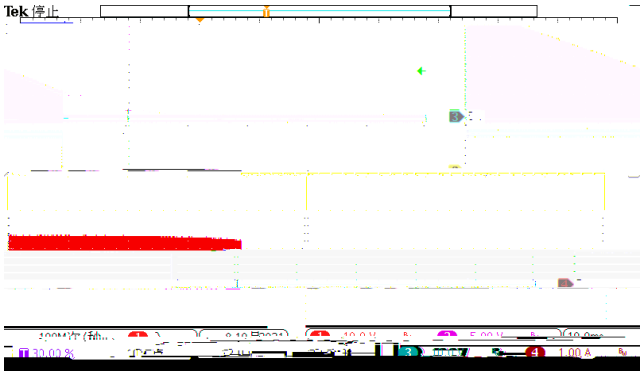

Figure 12. Power down(Iload=1A)

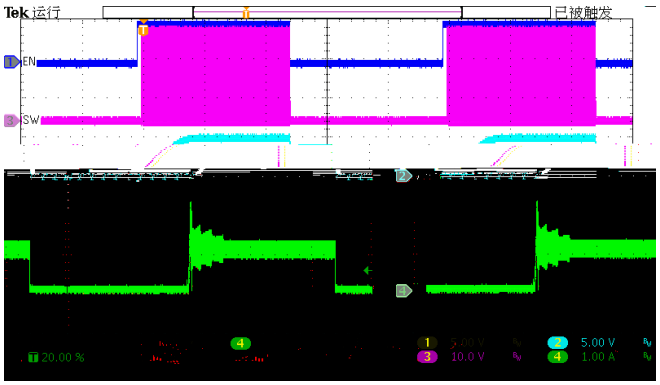

Figure 13.EN toggle (Iload=1A)

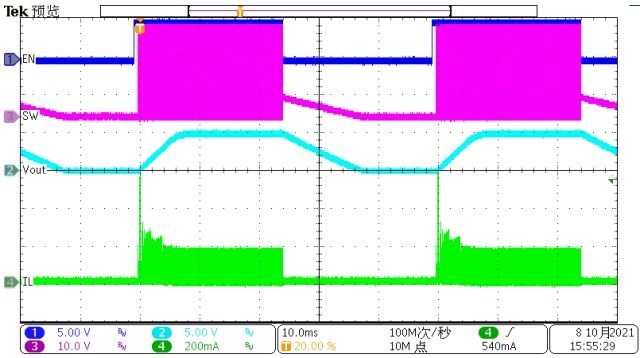

Figure 14. EN toggle (Iload=10mA)

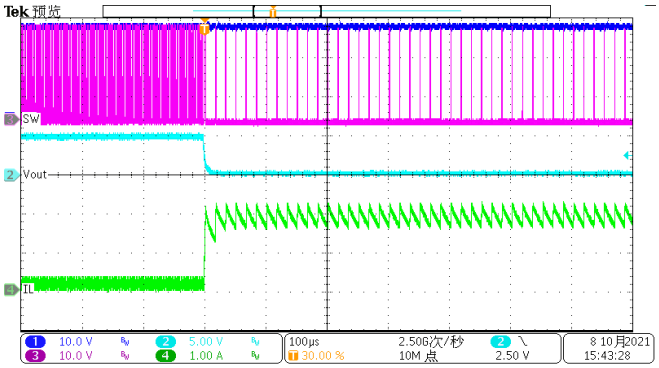

Figure 15. Over Current Protection(100mA to hard short)

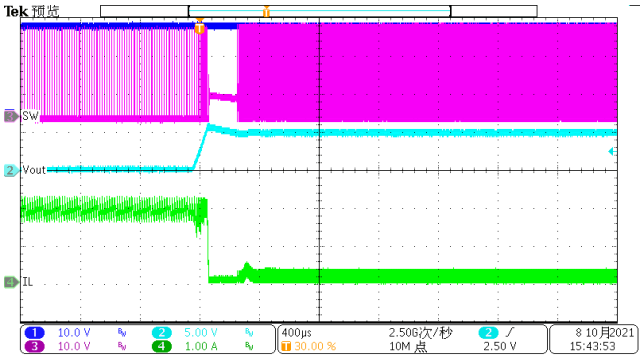

Figure 16. Over Current Release (hard short to 100mA)

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Vin=24V, Vout=5V, unless otherwise noted

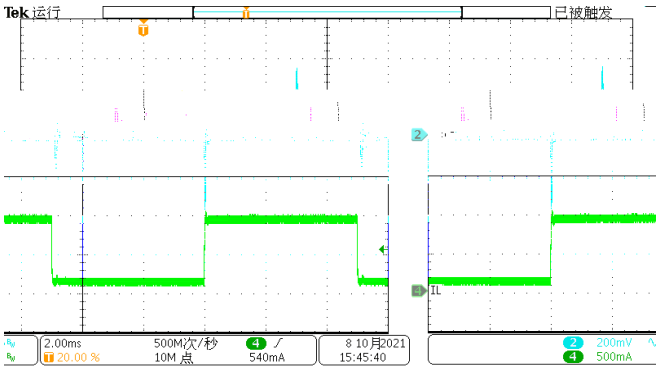

Figure 17. Load Transient (0.1A-0.9A, 1.6A/us)

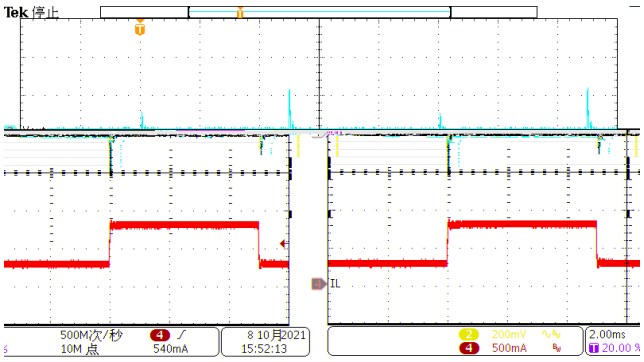

Figure 18. Load Transient (0.25A-0.75A, 1.6A/us)

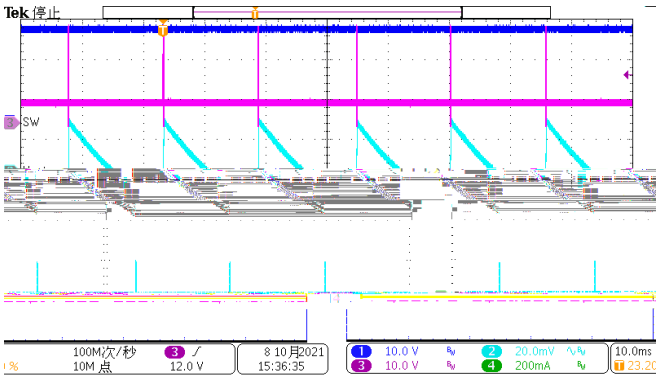

Figure 19. Output Ripple (Iload=0A)

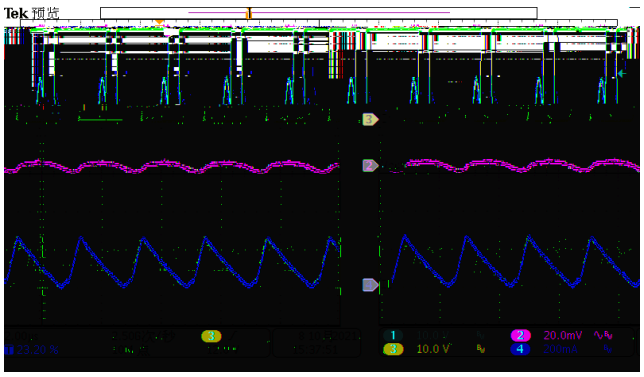

Figure 20. Output Ripple (Iload=100mA)

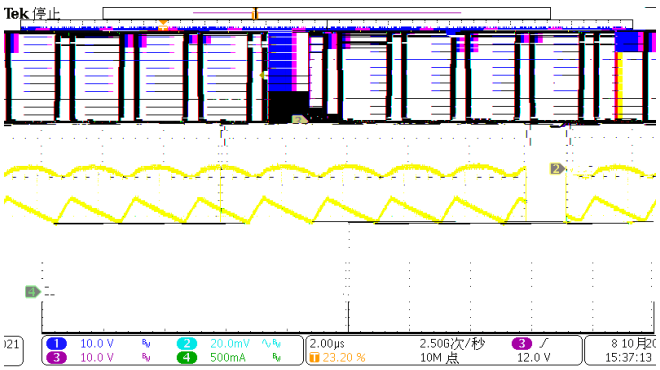

Figure 21. Output Ripple (Iload=1A)

Figure 22. Thermal, 24VIN, 5Vout, 1A

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The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential.

1. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize coupling.
2. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. UVLO adjust resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
5. Route BST capacitor trace on the other layer than top layer to provide wide path for topside ground.
6. The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

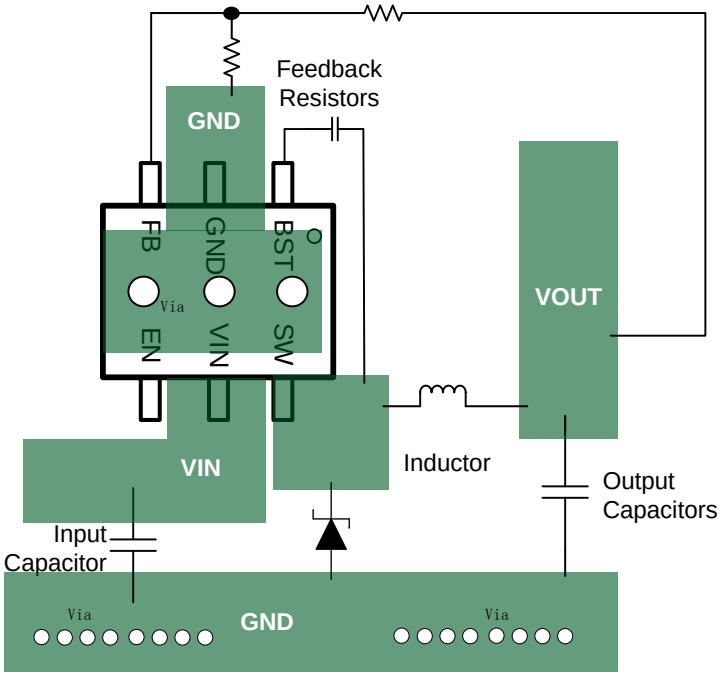

Figure 23. PCB Layout Example

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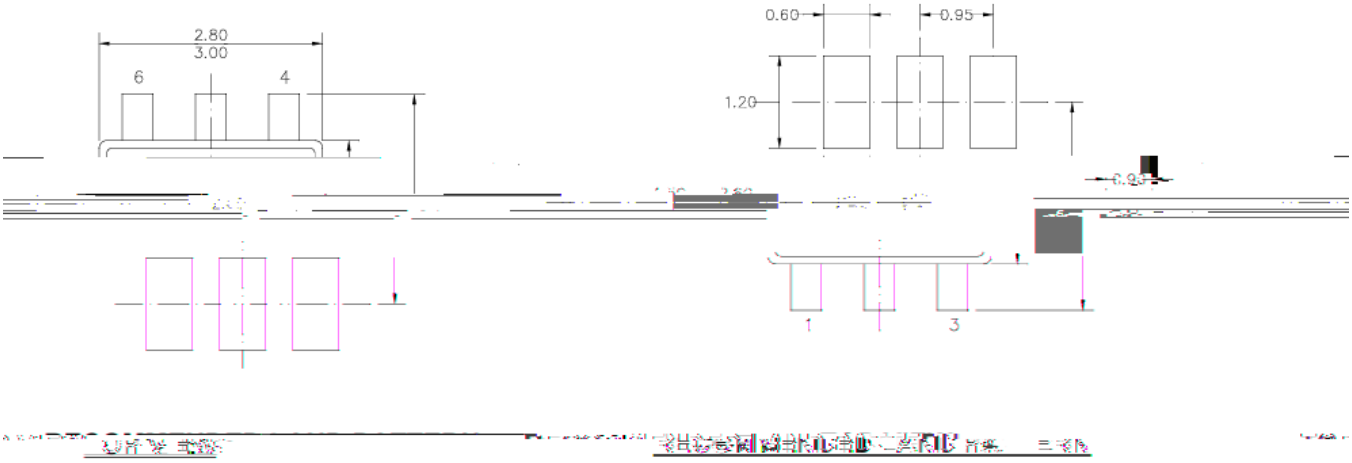
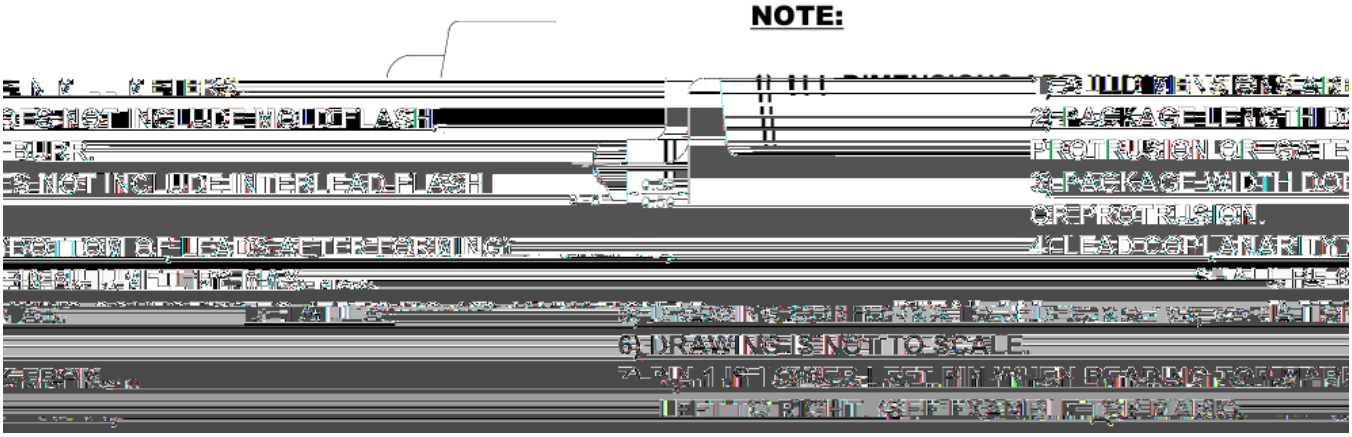


FRONT VIEW

SIDE VIEW

NOTE:



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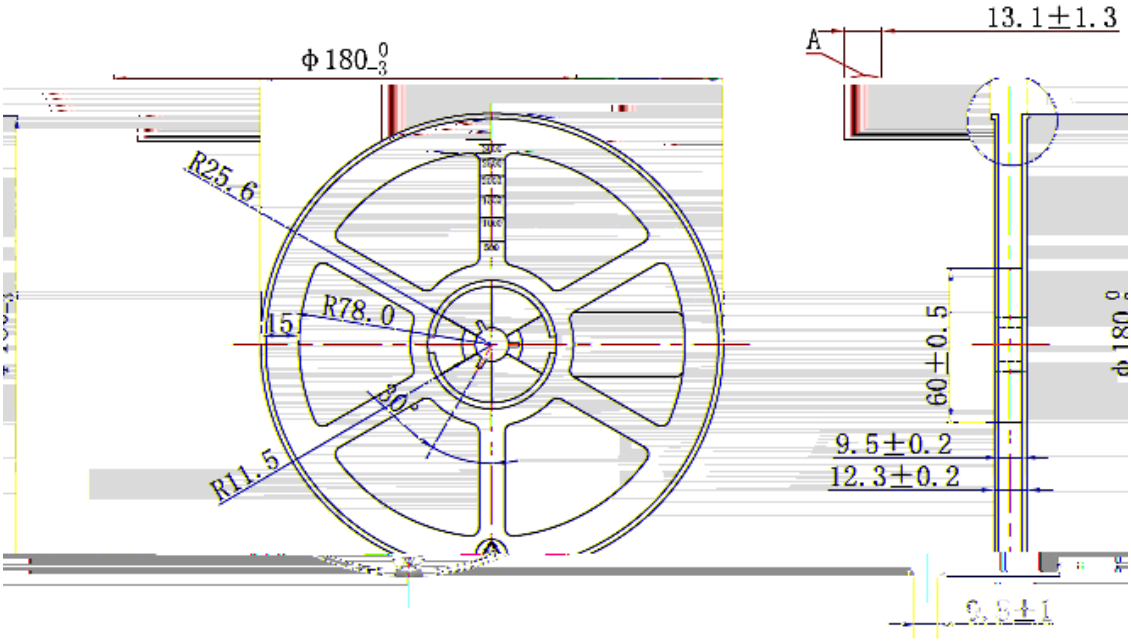

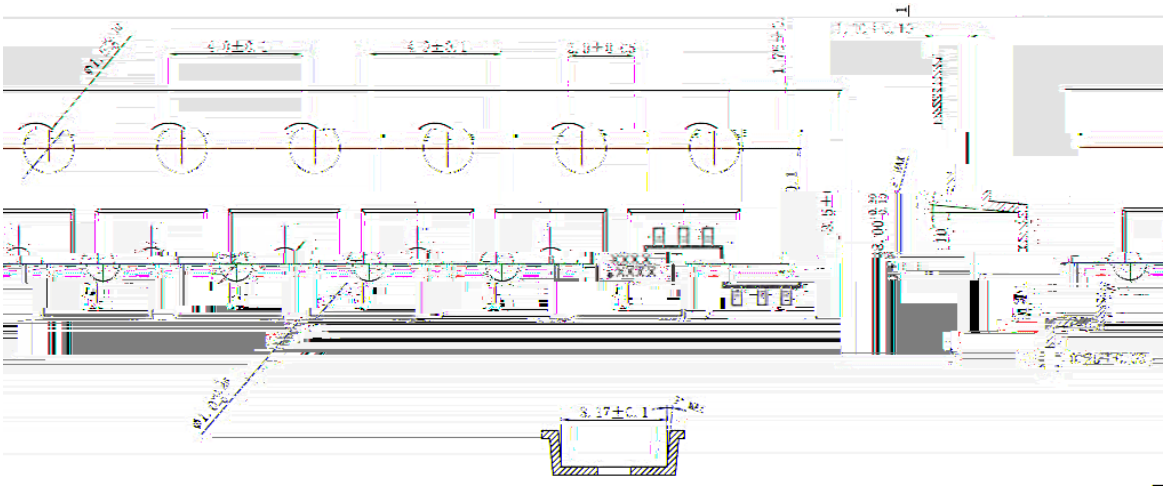

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