36V Vin Five Channels PMIC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with Ver.F Grade
- Synchronous LV Boost Converter VOUT4:
  - Up to 500mA Continuous Output Current
  - Output Voltage of 5V
- One Load Switch VOUT5:
  - Up to 800mA Continuous Output Current
- Programmable Power Sequencer for VOUT2, VOUT3, VOUT4 and VOUT5
- RESETB Output for System Management
- Simple/QA Watchdog
- Integrated Protection Features:
  - System Solution: The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.
  - Hardware Integrity up to Support ASIL-B System
  - ASIL-B Device Certification by TUV
  - BIST
- Up to 1MHz I2C Interface with Optional Packet Error Checking (PEC)
- Available in QFN-24 (4mm*4mm)

DESCRIPTION

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for SoCs in automotive and industrial radar applications.

The SCT61450S integrates one 3A HV Buck, two identical 2A LV Bucks, one 500mA LV Boost and one 800mA LV Load Switch. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter RESET state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61450S device has protection features such as thermal shutdown, short-circuit protection and over-voltage protection. Sleep mode reduces the total supply current to 0.85 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked during power up stage.

The device is available in a QFN-24(4mm*4mm) package with wettable flanks.

APPLICATIONS

- ADAS
- 77GHz Radar
- Safety MCU

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Add sleep mode and watchdog description, update thermal resistance and layout guideline, correct typo

Revision 1.2: Update SCT61450S-0001 VOUT2 to 1.15V, correct package marking, correct package description, add SS time limit in EC

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61450S-xxxxFDAR(1)	Tape & Reel	5000	1450S	24	FCQFN4x4-24L	1
SCT61450S-0001FDAR	Tape & Reel	5000	1450S	24	FCQFN4x4-24L	1

1) “xxxx” is the specific suffix code for different configuration, contact SCT for details

PART NUMBER	CHIP_ID	CONFIG_T1	CONFIG_EN	CONFIG_PU1	CONFIG_PU2	VOUT2	VOUT3	I2C ADDRESS
SCT61450S-0001FDAR	41h	00h	3Dh	00h	11h	07h 1.15V	0Eh 1.5V	38h

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
VOUT1	14	Voltage sense for the output of Buck1. The device regulates VOUT1 voltage to the setting value. PowerO002 Tu (Ou)0.7 (pge)0.7y.5 (B)3.3 (hei Tc 0 n

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT2}	LV buck2 output voltage range	0.8	2.35	V
V_{OUT3}	LV buck3 output voltage range	0.8	2.35	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-24	UNIT
R	Junction to ambient thermal resistance(1)	39.68	°C/W
JT	Junction-to-top characterization parameter	1.78	
JB	Junction-to-board characterization parameter(1)	3.26	
R	Junction to case (top) thermal resistance(1)	24.67	
R	Junction to board thermal resistance(1)	3.46	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61450S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61450S. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.5		36	V
$V_{IN\_UVLO\_RISING}$	Input UVLO rising threshold	VIN_START[1:0]=00b	3	3.2	3.4	V
		VIN_START[1:0]=01b	3.8	4	4.2	V
		VIN_START[1:0]=10b	4.8	5	5.2	V
		VIN_START[1:0]=11b	5.8	6	6.2	V
$V_{IN\_UVLO\_FALLING}$	Input UVLO falling threshold	VIN_STOP[1:0]=00b	2.5	2.8	3.1	V
		VIN_STOP[1:0]=01b	3.2	3.5	3.8	V
		VIN_STOP[1:0]=10b	4.2	4.5	4.8	V
		VIN_STOP[1:0]=11b	5.2	5.5	5.8	V
V_{IN_OVP}	Input OVP	V_{IN} rising	40	43	45	V
$V_{IN\_OVP\_HYS}$	Hysteresis			3		V
I_{SD}	Shutdown current	EN low		0.5	10	A
I_Q	Quiescent current from VIN	No load, FCCM, V_{OUT1} = 3.3V(1)		20		mA
		No load, PFM, V_{OUT1} = 3.3V(1)		1		mA
		Sleep mode, VOUT1 = 3.3V, no load, other rails disabled		0.5	2	mA
		All channels off via I2C		0.85	2	mA
VCC Power						
V_{CC}	Internal linear regulator		4.5	4.7	4.9	V
V_{CC_UVLO}	VCC UVLO	V_{CC} rising	2.6	2.8	3	V
$V_{CC\_UVLO\_HYS}$	Hysteresis			200		mV
V_{CCOV_THR}	VCC OV Threshold	V_{CC} rising	5	5.3	5.6	V
V_{CCOV_HYS}	Hysteresis			250		mV
IV_{CC}	VCC sourcing current limit	V_{CC} = 4.4V		70		mA
Enable and RESETB						
V_{EN_H}	Enable high threshold	V_{EN} ramping up		1.2	1.4	V
V_{EN_L}	Enable low threshold	V_{EN} ramping down	0.8	1.0		V
R_{EN_DOWN}	Enable pin pull-down resistance			2.1		
T_{RSTB}	RESETB pin holding time	RESETB_HT[1:0]=00b		10		ms
		RESETB_HT[1:0]=01b		20		
		RESETB_HT[1:0]=10b		30		
		RESETB_HT[1:0]=11b		40		
I_{RST_LKG}	Output-High leakage current				1	uA
V_{RST_L}	RESETB output low level	Sinking -2mA			0.2	V

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VOUT1 (HV Buck)						
V_{ACC1}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H1}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		75	150	
R_{DSON_L1}	Low-side MOSFET on-resistance			50	120	
I_{LIM_HS1}	High-side power MOSFET current limit		4.2	5.2	6.2	A
I_{LIM_LSP1}	Low-side power MOSFET positive current limit		3.2	4.2	5.2	A
I_{LIM_LSN1}	Low-side power MOSFET negative current limit		0.8	2	3.2	A
R_{DIS1}	Discharge resistance	Output disabled		100	200	
t_{ON_MIN1}	Minimum on-time			80		ns
$_{Phase1}$(1)	Switching phase			0		deg
VOUT2 (LV Buck)						
V_{S2}(1)	Supply voltage range		3		5.5	V
V_{ACC2}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H2}	High-side MOSFET on-resistance			65	150	
R_{DSON_L2}	Low-side MOSFET on-resistance			50	120	
I_{LIM_HS2}	High-side power MOSFET current limit		2.8	3.6	4.4	A
I_{LIM_LSP2}	Low-side power MOSFET positive current limit		2.2	3.2	4.2	A
I_{LIM_LSN2}	Low-side power MOSFET negative current limit		1	2	3	A
R_{DIS2}	Discharge resistance	Output disabled		50	100	
t_{ON_MIN2}	Minimum on-time			90		ns
$_{Phase2}$(1)	Switching phase			0		deg
VOUT3 (LV Buck)						
V_{S3}(1)	Supply voltage range		3		5.5	V
V_{ACC3}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H3}	High-side MOSFET on-resistance			65	150	
R_{DSON_L3}	Low-side MOSFET on-resistance			50	120	
I_{LIM_HS3}	High-side power MOSFET current limit		2.8	3.6	4.4	A

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Switching Frequency						
F_{SW}	LV Buck&Boost Switching frequency		1.98	2.2	2.42	MHz
F_{SW1}	HV Buck switching frequency	High frequency option	1.98	2.2	2.42	MHz
		Low frequency option	360	400	440	kHz
F_{FSS_RERIOD}	Frequency spread spectrum period	FSS_PERIOD[0]=0b		4.5		kHz
		FSS_PERIOD[0]=1b		10		
F_{FSS_RANGE}	Frequency spread spectrum in percentage of Fsw	FSS_RANGE[1:0]=00b		±5		%
		FSS_RANGE[1:0]=01b		±2.5		
		FSS_RANGE[1:0]=10b		±7.5		
		FSS_RANGE[1:0]=11b		±3.75		
Protection						
$V_{OVUVACC}$	OV/UV accuracy		-1.5		1.5	%
V_{OVTH}	Output over-voltage threshold for all outputs	PG1/2/3/4/5_SEL[1:0]=01, VOUT rising		106		%
		Hysteresis		2		%
V_{UVTH}	Output under-voltage threshold for all outputs	PG1/2/3/4/5_SEL[1:0]=01, VOUT falling		94		%
		Hysteresis		2		%
V_{DOVPTH}	Output deep over-voltage threshold for all outputs	DEEP_OVP_SEL[1:0]=00, VOUT rising	110	115	120	%
		Hysteresis		2		%
V_{DUVPTH}	Output deep under-voltage threshold for all outputs	DEEP_UVP_SEL[1:0]=00,VOUT falling	70	75	80	%
		Hysteresis		2		%
T_{HIC}(1)	Hiccup time			80		ms
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
	Hysteresis			20		°C
Low Power Interface						
R_{SLEEPB}	SLEEPB Input Pulldown	EN high		1.8		M
V_{SLEEPB_HI}	Threshold for SLEEPB pin	SLEEPB voltage rising		1.2	1.4	V
V_{SLEEPB_LO}		SLEEPB voltage falling	0.8	1		V
Watch Dog Interface						
V_{WDI_HI}	Threshold for WDI pin	WDI voltage rising		1.2	1.4	V
V_{WDI_LO}		WDI voltage falling	0.8	1		V
$T_{WDI\_DEG\_RISING}$	Deglitch time for WDI pin	WDI voltage rising		30		µs
T_{WD}	Watchdog timer accuracy		-10		10	%

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

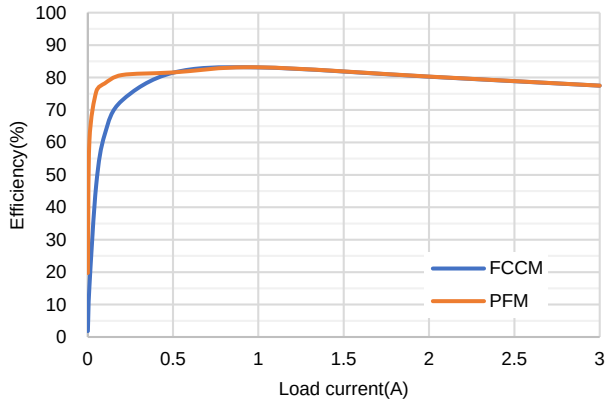
I2C Interface				
V_{IH}	High-level input voltage		1.2	V
V_{IL}	Low-level input voltage		0.4	V
V_{OL}	Low-level output voltage	I_{SINK}=4mA	0.4	V
F_{SCL}(1)	SCL clock frequency		1	MHz
T_{LOW}(1)	Low period of the SCL clock		500	ns
T_{HIGH}(1)	High period of the SCL clock		260	ns
T_{HD_STA}(1)	Hold time (repeated) START condition		260	ns
T_{SU_STA}(1)	Set-up time (repeated) START condition		260	ns
T_{HD_DAT}(1)	Data hold time		0	ns
T_{SU_DAT}(1)	Data set-up time		50	ns
T_R(1)	Rise time of both SCL and SDA signals		120	ns
T_F(1)	Fall time of both SCL and SDA signals		120	ns
T_{SU_STO}(1)	Set-up time for STOP condition		260	ns
CB(1)	Capacitive load for each bus line		550	pF

(1) Guaranteed by sample and design characterization, not tested in production.

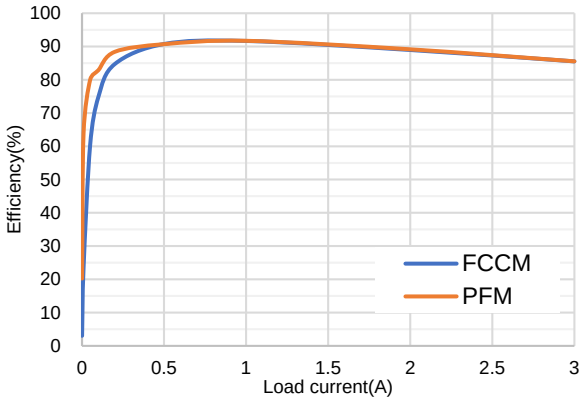
 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

TYPICAL CHARACTERISTICS

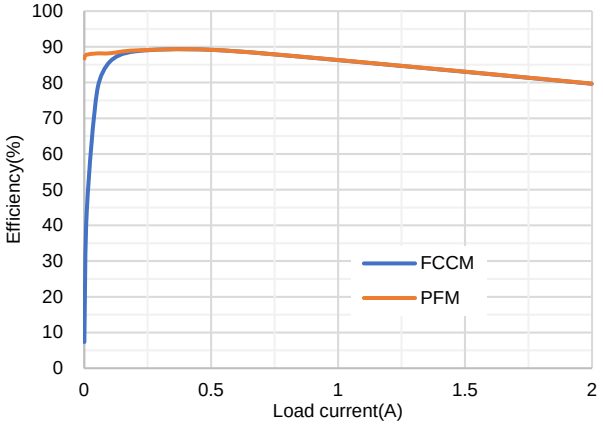
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



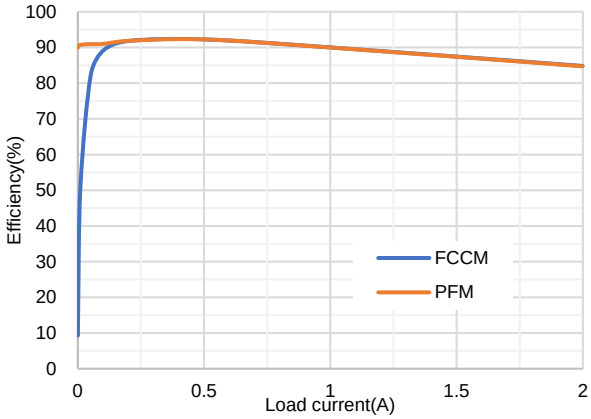
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.2MHz



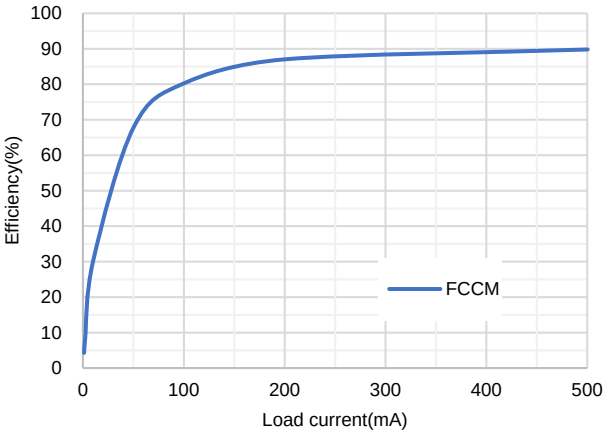
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



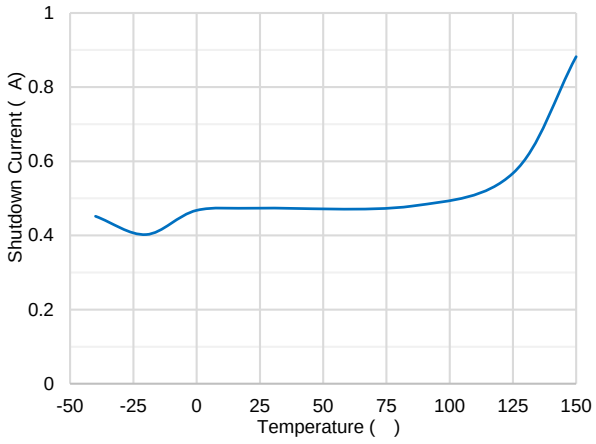
Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V



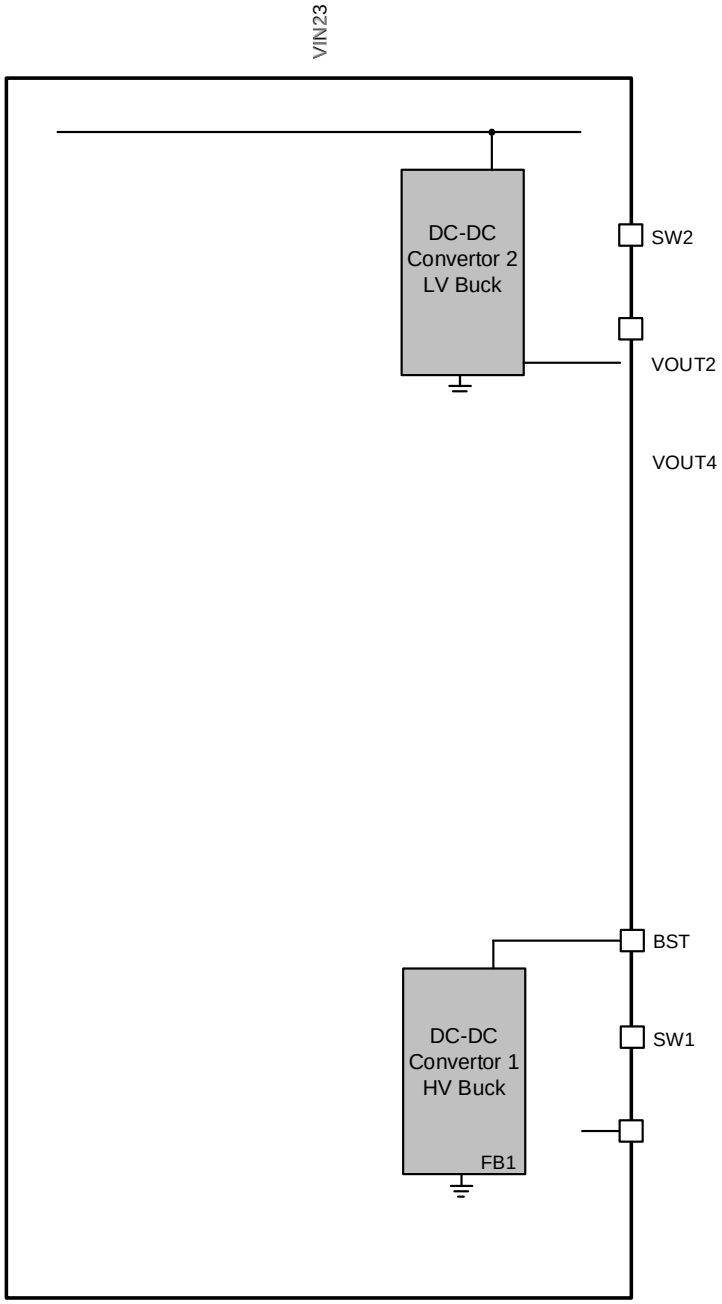
Boost Efficiency vs. Load Current, V_{OUT4}=5V



Shutdown Current vs. Temperature

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

FUNCTIONAL BLOCK DIAGRAM 2



 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

OPERATION

Overview

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for SoCs in automotive and industrial radar applications. The SCT61450S integrates one 3A HV Buck, two identical 2A LV Bucks, one 500mA LV Boost and one 800mA LV Load Switch. Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61450S device has protection features such as thermal shutdown, short-circuit protection and over-voltage/under-voltage protection. Sleep mode reduces the total supply current to 1 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked before power up stage. Safety features ensure compliance with ISO26262 standard and functional safety up to ASIL-B level.

Operating State Machine

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Table 1. Sate and Function Matrix Table

State	Function											
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LV BOOST4	LOAD SWITCH5	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LOADOTP	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LBIST	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEPSAFE	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
ABIST	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
POWERUP	ON	OFF	OFF	UP	UP	UP	UP	UP	OFF	ON	ON	ON
NORMAL	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON
RESET	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	ON
SLEEP	OFF	OFF	OFF	ON	ON /OFF	ON /OFF	ON /OFF	ON /OFF	ON/OFF	ON	ON	ON
RECOVER	ON	OFF	OFF	ON	ON/UP	ON/UP	ON/UP	ON/UP	ON	ON	ON	ON
RCVRST	ON	OFF	OFF	ON	ON/UP	ON/UP	ON/UP	ON/UP	OFF	ON	ON	ON

Table 2. Sate and Functional Pin Matrix Table

State	SLEEPB	RESETB
IDLE	Tri-state	Tri-state
LOADOTP	X	LOW
DEEPSAFE	X	LOW
ABIST	X	LOW
POWERUP	X	LOW
NORMAL	HIGH	HIGH

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

- VOUT5's output is out of deep OV/UV protection range or OCP
- Tj reaches Thermal Shutdown Point
- VIN/EN UVLO
- VCC OVP
- VIN OVP
- RESETB Stuck
- Loss of ground

ABIST State

To ensure safety mechanism work well, the device will check through all critical analog comparators before output start-up. If ABIST check is failed, the device will go back to DEEPSAFE state. ABIST will be implemented every time SCT61450S enter ABIST state, the device will transit to POWERUP state once ABIST is passed. Any ABIST failure will be recorded in register **SYS_STATE**.

POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

rail on, other rails are optional depending on register **CONFIG_ENLP**. Most unnecessary circuits will turn off to save power consumption. Deep safe event is still valid to provide protection. Note the RESETB pin is still high during this state to keep MCU alive. Once SLEEPB pin is pulled high longer than deglitch time, the device will exit from sleep mode and go to RECOVER state. The rest channels will then recover.

RECOVER State

Once the device is awake from sleep mode, the RECOVER state is an intermediate state before device go back to NORMAL state. The channels which are disabled in SLEEP state will start up according to programmed turn on delay. After all output are built up successfully, the device will then enter NORMAL state. If there is reset event during RECOVER state, the device will go to RCVRST state.

RCVRST State

RCVRST state is extra reset state to assert RESETB pin, other rails will still start up in programmed sequence. This state aims to provide possible reset events including OV/UV and watchdog detection for those continuously enabled rails. The device will go back to RECOVER state automatically after once the holding time is expired and no reset event.

VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplify the system design.

High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks and one boost employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4/5.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180° phase-shifted clock.

The VOUT4 is a LV synchronous boost converter also power by VOUT1. It's regulated at 5V with up to 500mA continuous current.

The VOUT5 is a load switch output powered by VOUT1, the integrated MOSFET on-resistance is 100

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

Deep Over Voltage Protection

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_UVP_SEL[1:0]**.

Thermal Shutdown

The thermal shutdown protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175 , the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 155 , the device will restart with internal soft start phase.

Over Current Protection (OCP)

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When peak current point is kicked for continuous 32 times, the converter stops switching, the device will jump to DEEPSAFE state. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

For the boost, the device provides a load disconnect function, which completely disconnects the output from the input during overload. Then output short to ground fault is protected.

Frequency Spread Spectrum

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Sleep Mode

The SCT61450S integrates an ultra power-saving mode with VOUT1 on. When in sleep mode, the disabled channels will shutoff and the alive channels will operate under PFM to further improve efficiency. Only after all disabled channels shutoff, pulling SLEEPB pin high can wake up the device and exit sleep mode. It can coordinate with MCU to achieve sleep mode system with extremely low consuming current from battery. If **LOWPOWER_EN[0]**=0, the device will ignore the inputs from SLEEPB pin and never enter sleep mode.

There are two cases for the device to enter sleep mode: a) **LOWPOWER_EN[0]**=0 in OTP setting, the MCU must set bit **LOWPOWER_EN[0]**=1 in register **CONFIG_ENLP** to enable sleep mode first, then pull SLEEPB pin low. When the device exit sleep mode, the bit **LOWPOWER_EN[0]** will be reset automatically. b) **LOWPOWER_EN[0]**=1 in OTP setting, pull SLEEPB pin low will bring device to sleep mode directly. When the device exit sleep mode, the bit **LOWPOWER_EN[0]** will also be reset automatically. Master must set bit **LOWPOWER_EN[0]**=1 to enter sleep mode again.

If bit **WD_EN[0]=1** when entering sleep mode, watchdog window timer counts during sleep mode. The device will exit sleep mode once a WD failure occurs and enter RCVRST state. An appropriate window length setting can help the MCU be monitored by watchdog over the duration of sleep mode. Besides, watchdog expiration error can increase fault coverage even the MCU can't send watchdog response.

To avoid spike and noise on SLEEPB pin, the pin rising/falling deglitch time and blank time can be configured by register **CONFIG_SLEEPB**.

Watchdog

During NORMAL state, the watchdog can monitor the MCU with programmable cycle. Everytime the device enters NORMAL state and RESETB pin is released, the watchdog will be activated if WDDIS pin is low and bit **WD_EN[0]**=1b. There will be extension cycles if **WD_EN[0]**=1b when entering NORMAL state, which is used to wait MCU's program loading process and can be configured by bit **WD_1UD[2:0]**. During the close window of first update extension, any WDI or **WD_KEY** signals will be ignored and WD error counter keeps zero.

Simple Watchdog

If **WD_MODE[0]** = 1, the device will implement simple watchdog, the MCU should provide trigger pulse to WDI pin or write any byte to specific register **WD_KEY** within the open window. The length of open window and closed window can be configured by I2C. A correct watchdog trigger will restart the whole window cycle immediately. Giving pulse or writing byte to register **WD_KEY** during the closed window will result in **WD_UV[0]** violation and will restart the whole window cycle immediately. If MCU doesn't send high pulse or write byte to **WD_KEY** before the whole window is expired, **WD_EXP[0]** violation occurs. Any violation will make the WD error counter plus one. When WD error counter reaches the **WD_FAIL_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

QA Watchdog

If **WD_MODE[0]** = 0, the device will implement Question and Answer (QA) watchdog and signals on WDI pin are ignored. In QA watchdog mode, MCU should read register **WD_KEY** to get the answer through I2C. Then MCU response the watchdog in open window through writing the specific answer to register **WD_KEY**. A correct watchdog trigger will refresh the whole window cycle immediately and the **WD_KEY** register being updated. Writing the incorrect answer to the **WD_KEY** will result in the value written being ignored and a **WD_LFSR[0]** violation. Writing the correct response during a closed window will result in the write being ignored and a **WD_UV[0]** violation. If MCU doesn't write byte to **WD_KEY** and the whole window is expired, **WD_EXP[0]** violation occurs. LFSR polynomial: x8 + x6 + x5 + x4 + 1. Any violation except **WD_LFSR[0]** violation will make the WD error counter plus one. When WD error counter reaches the **WD_FAIL_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

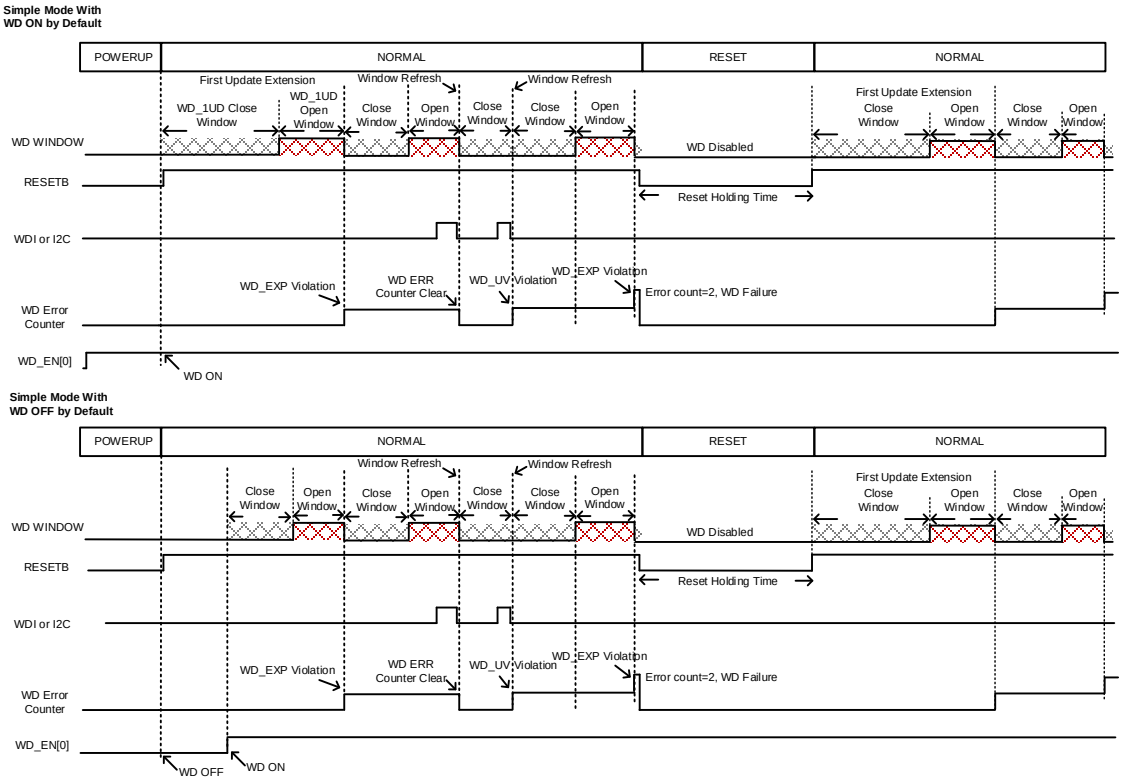


Figure 3a. Simple Watchdog Error Timing

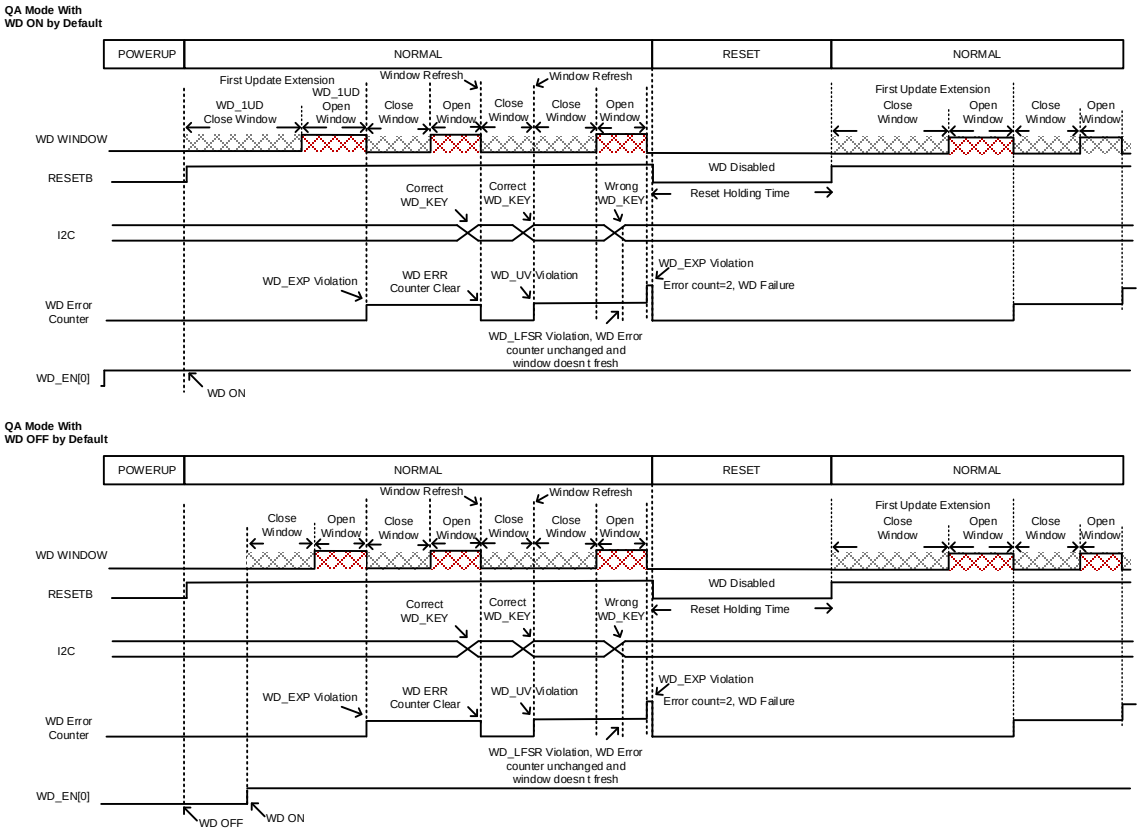


Figure 3b. QA Watchdog Error Timing

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

I2C Interface

The SCT61450S integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61450S is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61450S supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

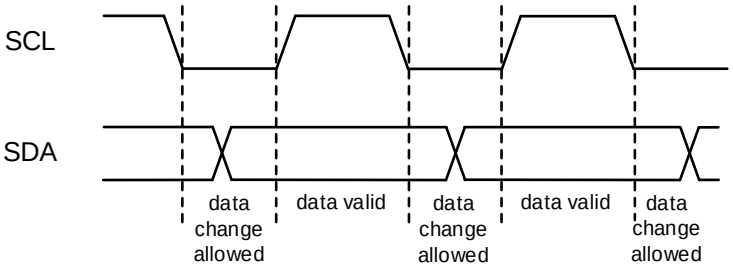


Figure 4. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

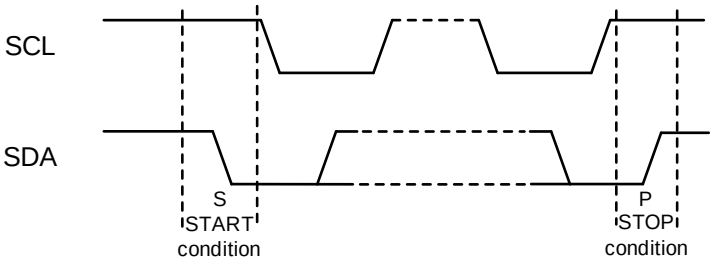


Figure 5. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61450S will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

Packet Error Checking (PEC)

The SCT61450S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated over the entire message from the first START condition. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC_EN** in register **CONFIG_FSS**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 6 illustrates the proper format for one frame.

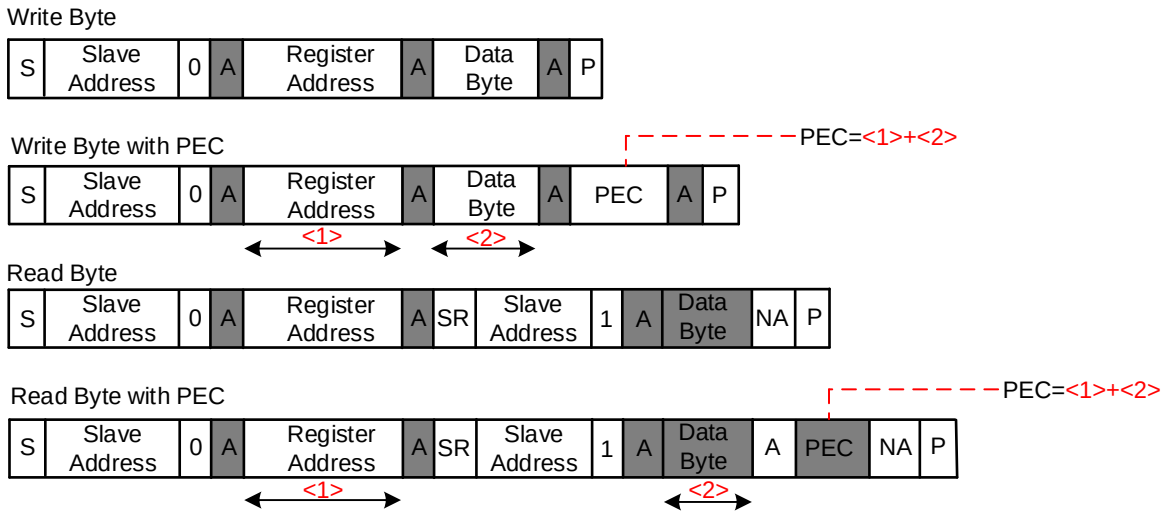


Figure 6. Transmission Data Format Diagram

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

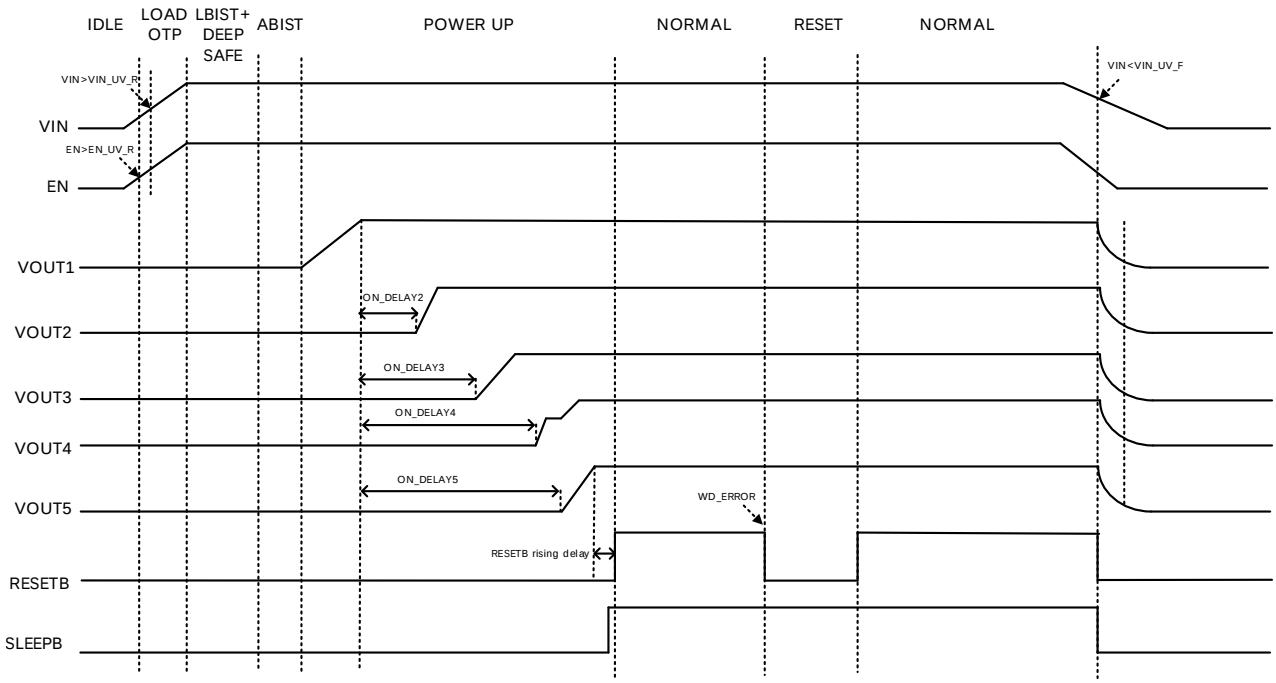
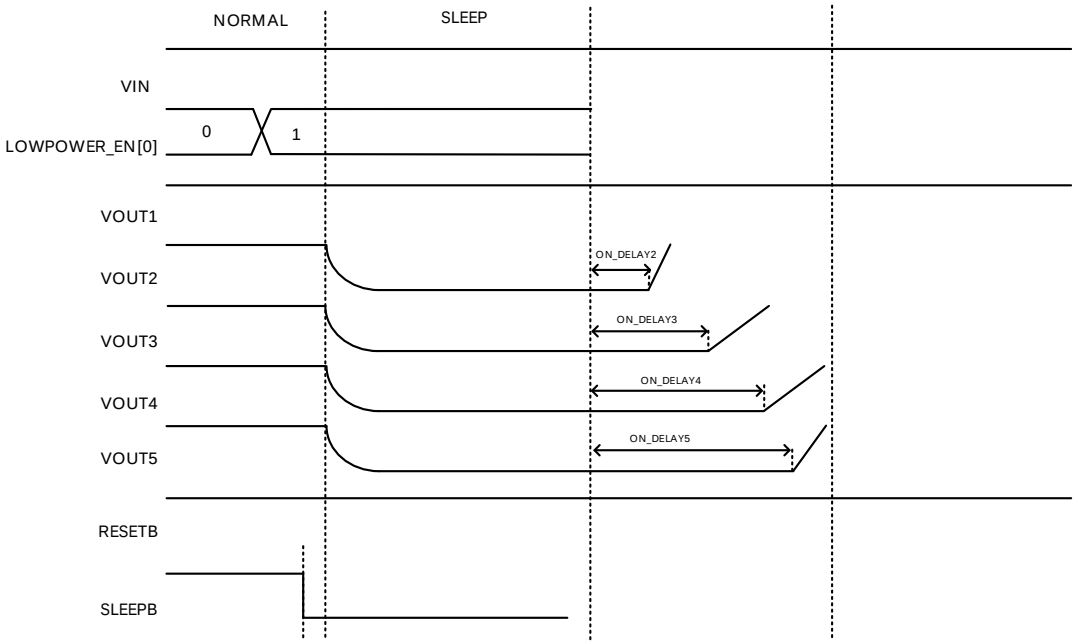


Figure 7. Power on Sequence



 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

APPLICATION INFORMATION

Typical Application

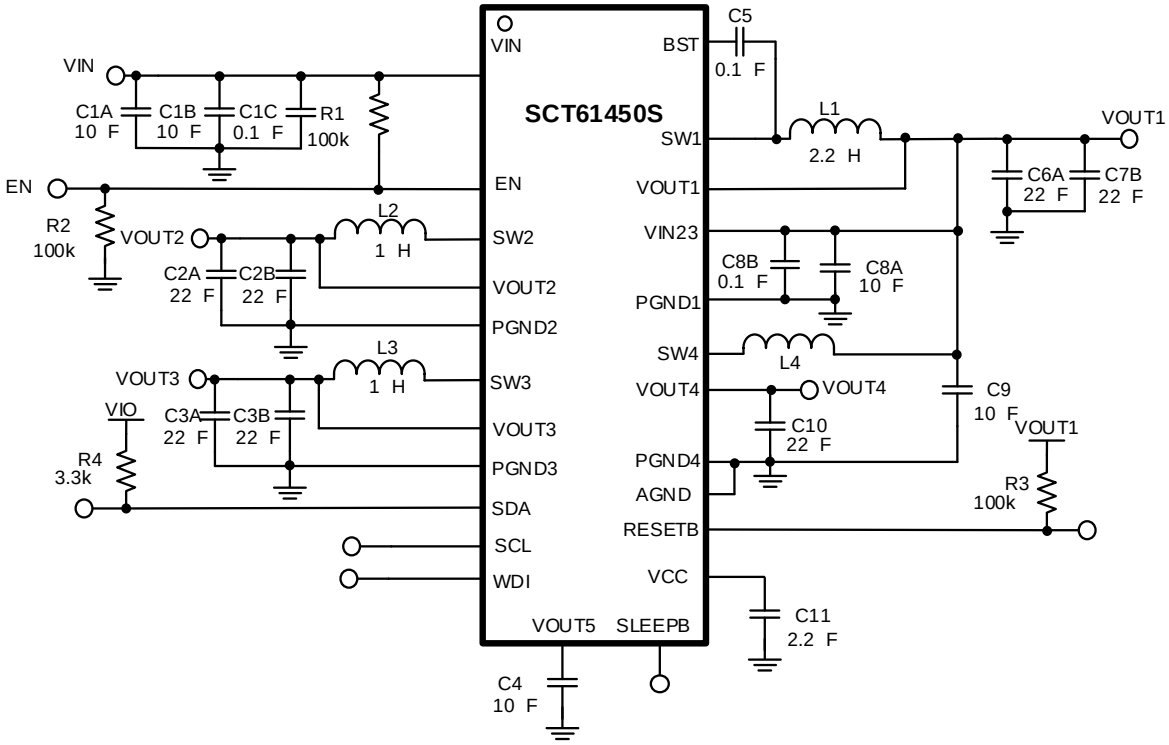


Figure 9. Application Schematic, 3.5V to 36V, PMIC Regulator at 2.2MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 3.5V to 36V
Output Voltage	VOUT1: 3.3V VOUT2: 1.1V VOUT3: 1.5V VOUT4: 5V VOUT5: 3.3V
Maximum Output Current	VOUT1: 3A (in total) VOUT2: 2A VOUT3: 2A VOUT4: 500mA VOUT5: 800mA
Switching Frequency	2.2MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 5mV VOUT3: 5mV VOUT4: 20mV VOUT5: 2mV

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Under Voltage Lock-Out

An external voltage divvvadeout 0 7.98(ut 0366572(67857.8)Tj2EMC 2 -0 0 10.02 54 63702.22678572( )Tj ET q1 Tc -0.039

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$= + \frac{}{2} \quad (5)$$

$$= \sqrt{( )^2 + \frac{1}{12} ( )^2} \quad (6)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

For a boot converter, the peak-to-peak ripple current in the inductor I_{LPP} can be calculated as

$$_{-} = \frac{1}{\times (\frac{1}{-} + \frac{1}{}) \times} \quad (7)$$

Where

- I_{LPP_BOOST} is the inductor peak-to-peak current of boost
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Calculate the inductor DC current as in equation 8

$$= \frac{\times}{\times} \quad (8)$$

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as

$$= + \frac{}{2} \quad (9)$$

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

$$= \frac{}{} \left(1 - \frac{}{}\right) \quad (10)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$= 0.5 \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta = \frac{}{} \left(1 - \frac{}{}\right) \quad (12)$$

For the boost converter power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 10 input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

ST pin and SW1 pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 13 desired.

$$\Delta \quad = \frac{(\quad - \quad)}{8 \quad ^2} \quad (13)$$

Where

- $_{OUT\_BUCK}$ is the output voltage ripple of buck converter
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

For boost converter, typically, a 10 amic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. From the required output voltage ripple, use the below equation to calculate the minimum required effective capacitance

$$\Delta \quad - \quad = \frac{(\quad - \quad - \quad) \times}{\times \quad \times} \tag{14}$$

where

- $_{OUT\_BOOST}$ is output voltage ripple caused by charging and discharging of the output capacitor of boost
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- f_{SW} is the converter switching frequency.

Table 3. Recommended BOM for Typical Application

Output Rail	Frequency (MHz)	L (uH)	Input Capacitor (uF)	Output Capacitor (uF)
Buck1	2.2	2.2	2 x 10+1 x 0.1	2 x 22
Buck2	2.2	1	10+1 x 0.1	2 x 22
Buck3	2.2	1		2 x 22
Boost4	2.2	1	10	22
Loadswitch5	-	-	-	10
VCC	-	-	-	2.2

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=3.3V,unless otherwise noted

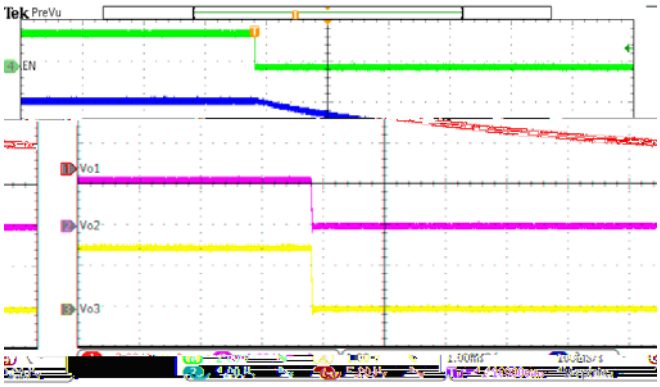


Figure 17. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

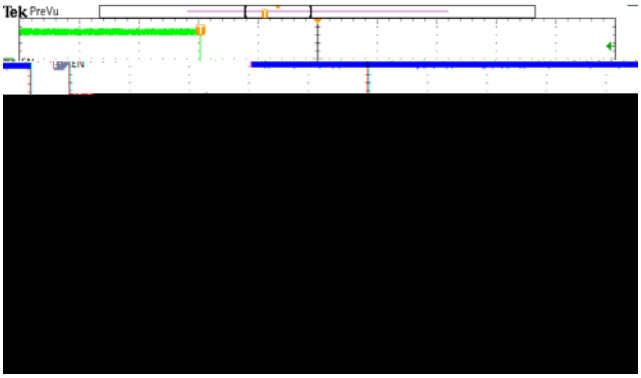


Figure 18. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

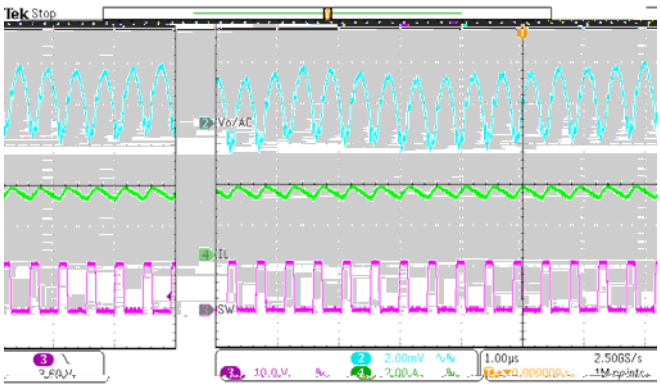


Figure19. Buck1 Steady State (Io1 = 3A)

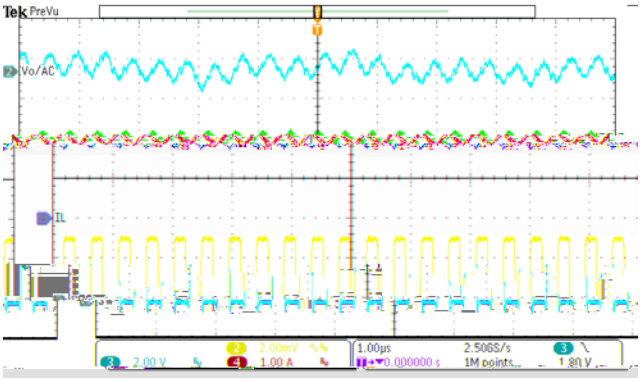


Figure 20. Buck2 Steady State (Io2 = 2A)

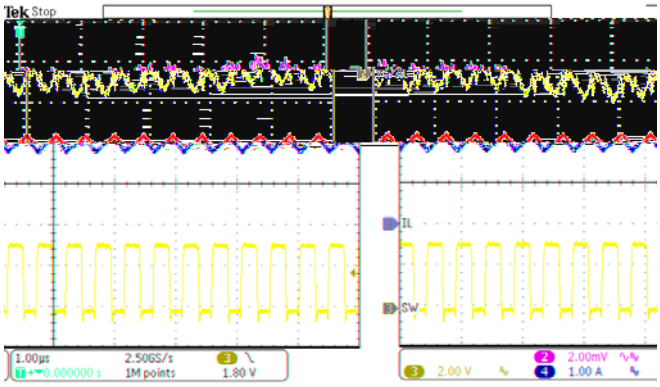


Figure 21. Buck3 Steady State (Io3 = 2A)

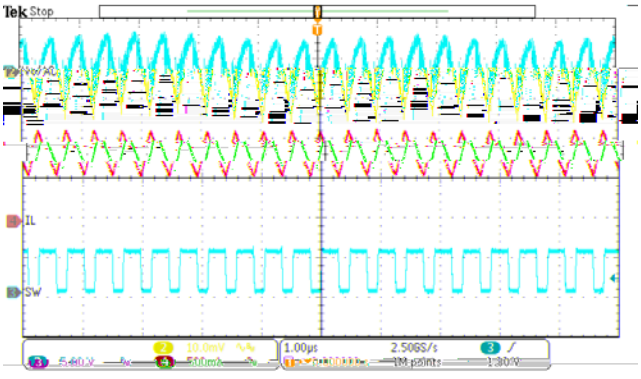


Figure 22. Boost4 Steady State (Io4 = 500mA)

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=3.3V,unless otherwise noted

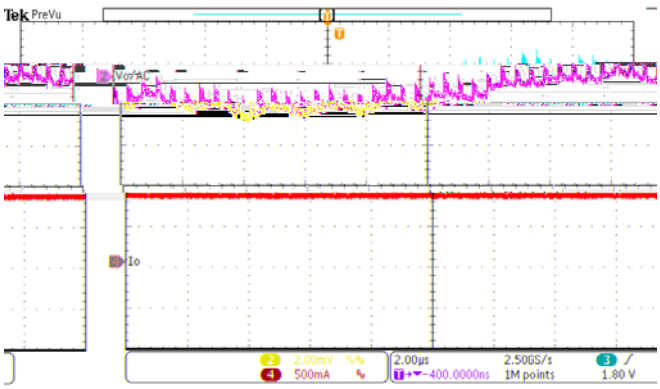


Figure 23. Loadswitch Steady State (Io5 = 800mA)

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impendence.
3. Place a low ESR ceramic capacitor as close to VIN1 and VIN23 pin and the ground as possible to reduce parasitic effect.

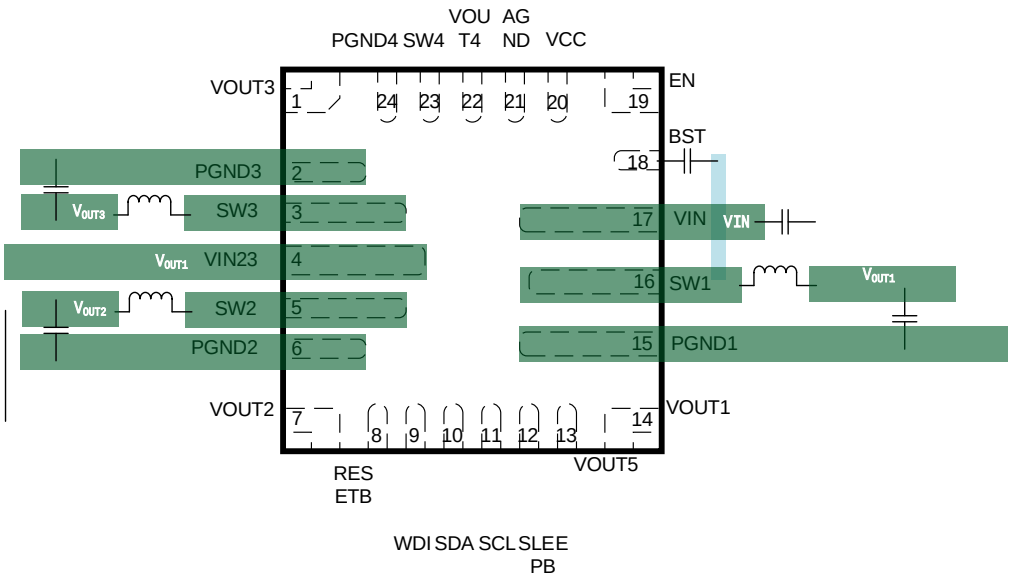
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. For achieving better thermal performance, a four-layer layout is strongly recommended.



 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Register Map

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C LOCK	WD LOCK
0x00	CHIPID	-	Y	N	N
0x01	CONFIG_FSS	70h	Y	Y	N
0x02	CONFIG_T1	00h	Y	Y	N
0x03	CONFIG_T2	1Fh	Y	Y	N
0x05	CONFIG_EN	3Dh	Y	Y	N
0x06	CONFIG_PU1	00h	Y	Y	N
0x07	CONFIG_PU2	11h	Y	Y	N
0x08	RSTMAP	3Fh	Y	Y	N
0x0A	STATUV	00h	N	N	N
0x0B	STATOV	00h	N	N	N
0x0C	STATOFF	00h	N	N	N
0x0D	STATD	00h	N	N	N
0x0E	STATWD	00h	N	N	N
0x0F	VOUT2	07h	Y	Y	N
0x10	VOUT3	0Eh	Y	Y	N
0x11	CONFIG_MISC	00h	Y	Y	N
0x12	CONFIG_PFM	00h	Y	Y	N
0x13	CONFIG_WD1	87h	Y	N	Y
0x14	CONFIG_WD2	0Eh	Y	N	Y
0x15	CONFIG_WD3	13h	Y	N	Y
0x16	WD_KEY	AAh	Y	N	N
0x17	WD_LOCK	00h	N	N	N
0x18	CONFIG_ENLP	2Ch	Y	Y	N
0x19	CONFIG_PGSEL1	01h	Y	Y	N
0x1A	CONFIG_PGSEL2	55h	Y	Y	N
0x1B	CONFIG_SLEEPB	30h	Y	Y	N
0x1C	I2C_LOCK	01h	N	N	N
0x22	SYS_STATE	00h	N	N	N

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

				11: Scale =5ms. Delay ranges from 0-75ms

CONFIG_T2 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	*RESERVED*	R	/	/
[5]	DF_SCALE	W/R	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Analog Filter Time = 10µs. Added Digital Filter Time =DF[4:0] x 2µs, when DF_SCALE=0, =DF[4:0] x 10µs, when DF_SCALE=1.
[4:0]	DF	W/R		

CONFIG_EN [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	*RESERVED*	R	/	/
[5]	EN5	W/R	Enable for Load Switch OUT5. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[4]	EN4	W/R	Enable for LV BOOST OUT4. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[3]	EN3	W/R	Enable for LV BUCK OUT3. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[2]	EN2	W/R	Enable for LV BUCK OUT2. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[1]	RESERVED	R	/	/
[0]	EN_ALL	W/R	Enable for all channel	0 = Output Disabled 1 = Output Enabled

CONFIG_PU1 [7:0]				
ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	ON_DELAY5	W/R	OUT5 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY5} = ON_DELAY5[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY5} = ON_DELAY5[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY5} = ON_DELAY5[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY5} = ON_DELAY5[3:0] x 5ms
[3:0]	ON_DELAY4	W/R	OUT4 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY4} = ON_DELAY4[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY4} = ON_DELAY4[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY4} = ON_DELAY4[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY4} = ON_DELAY4[3:0] x 5ms

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

STATUV [7:0]			
ADDRESS: 0x0A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	UV	Read Clear	UV Comparator Status for all channels with Digital Filter.
[6]	RESERVED	R	/
[5]	UV_WARN5V	Read Clear	UV warning for OUT5, Digital Filter is not included

[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

STATOFF [7:0]				
ADDRESS: 0x0C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	OFF5	Read Clear	OFF Comparator Status for OUT5	0 = OUT5 is above OFF threshold 1 = OUT5 is below OFF threshold
[4]	OFF4	Read Clear	OFF Comparator Status for OUT4	0 = OUT4 is above OFF threshold 1 = OUT4 is below OFF threshold
[3]	OFF3	Read Clear	OFF Comparator Status for OUT3	0 = OUT3 is above OFF threshold 1 = OUT3 is below OFF threshold
[2]	OFF2	Read Clear	OFF Comparator Status for OUT2	1.4 ( )0.6 (O)0.6 (U)-1.6 (T)7.2 (3)]TJ 0 T

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

STATWD [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RESETB_STAT	R	RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.	0 = RESETB is low 1 = RESETB is high
[4]	WD_OPEN	R	Watchdog Open Window. This bit indicates that it is permissible to update the watchdog. This bit shows real-time status.	0 = Watchdog update not open 1 = Watchdog ok to update
[3]	WD_ERR	R	Watchdog ERROR for 1 time or 2 times (config by WD_FAIL_CNT), LFSR mismatch is not included	0 = No error detected 1 = Error detected
[2]	WD_LFSR	Read Clear	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read
[1]	WD_UV	Read Clear	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.	0 = No violation detected 1 = Watchdog updated too early
[0]	WD_EXP	Read Clear	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT2	W/R	OUT2 Voltage Setting	VOUT2 = OUT2[4:0] x 50mV + 0.8V (0.8V to 2.35V)

VOUT3 [7:0]				
ADDRESS: 0x10				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT3	W/R	OUT3 Voltage Setting	VOUT3 = OUT3[4:0] x 50mV + 0.8V (0.8V to 2.35V)

CONFIG_MISC [7:0]				
ADDRESS: 0x11				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4]	VIN_OVP_EN	W/R	Enable of VIN OVP. When VIN>43V, part enter DEEPSAFE mode.	0 = Disabled 1 = Enabled
[3:2]	VIN_START	W/R	VIN start threshold at VIN rising	00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V
[1:0]	VIN_STOP	W/R	VIN stop threshold at VIN falling	00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

CONFIG_PFM [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RESERVED	R	/	/
[3]	PFM4	W/R	BOOST4 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[2]	PFM3	W/R	BUCK3 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[1]	PFM2	W/R	BUCK2 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[0]	PFM1	W/R	BUCK1 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM

CONFIG_WD1 [7:0]				
ADDRESS: 0x13				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WD_MODE	W/R	Watchdog Mode Selection	0 = QA watchdog enabled

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

[2:0]	WD_1UD	W/R	First Update Extension. Sets the number of extra watchdog window cycles after POR to the normal watchdog window.	t1STWD_CLOSE = tWD_CLOSE x (WD_1UD [2:0] + 1) t1STWD_OPEN = tWD_OPEN x (WD_1UD [2:0] + 1)

WD_KEY [7:0]				
ADDRESS: 0x16				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	WD_KEY	W/R	Watchdog Key.	The current key can be read from this register. To update the watchdog, the next value in the sequence must be written to this register. If configured as a simple windowed watchdog, writing any value to the WDKEY register will refresh the watchdog and the value written will be ignored. If configured as a QA watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in QA mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in QA mode during a closed window will result in the write being ignored and a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]				
ADDRESS: 0x17				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	*RESERVED*	R	/	/
[0]	WDLOCK	W/R	Watchdog Lock Protection	0 = Watchdog configuration registers are writeable 1 = Watchdog configuration registers are read-only

CONFIG_ENLP [7:0]				
ADDRESS: 0x18				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	EN5_LP	W/R	Low power mode enable control for Load Switch OUT5.	0 = Output enabled in low power mode 1 = Output disabled low power mode
[4]	EN4_LP	W/R	Low power mode enable control for LV BOOST OUT4.	0 = 42 104.5 34.-0.put disabled5T Q

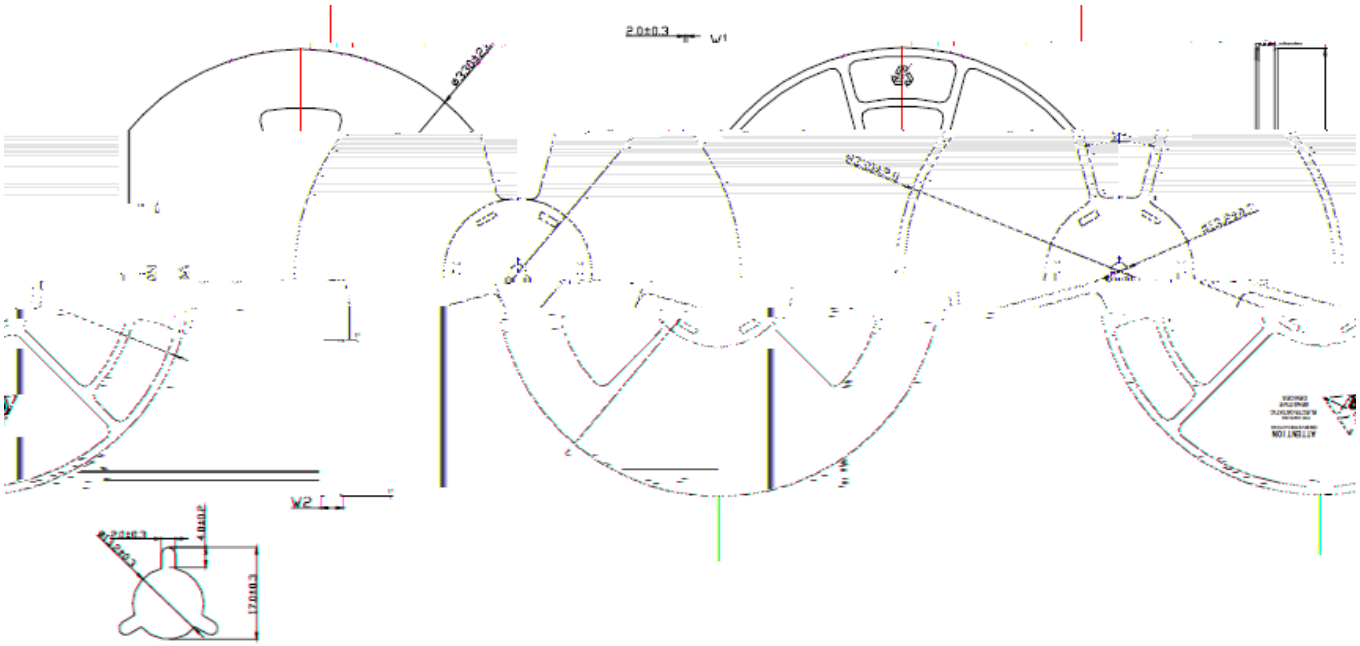
 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

PACKAGE INFORMATION

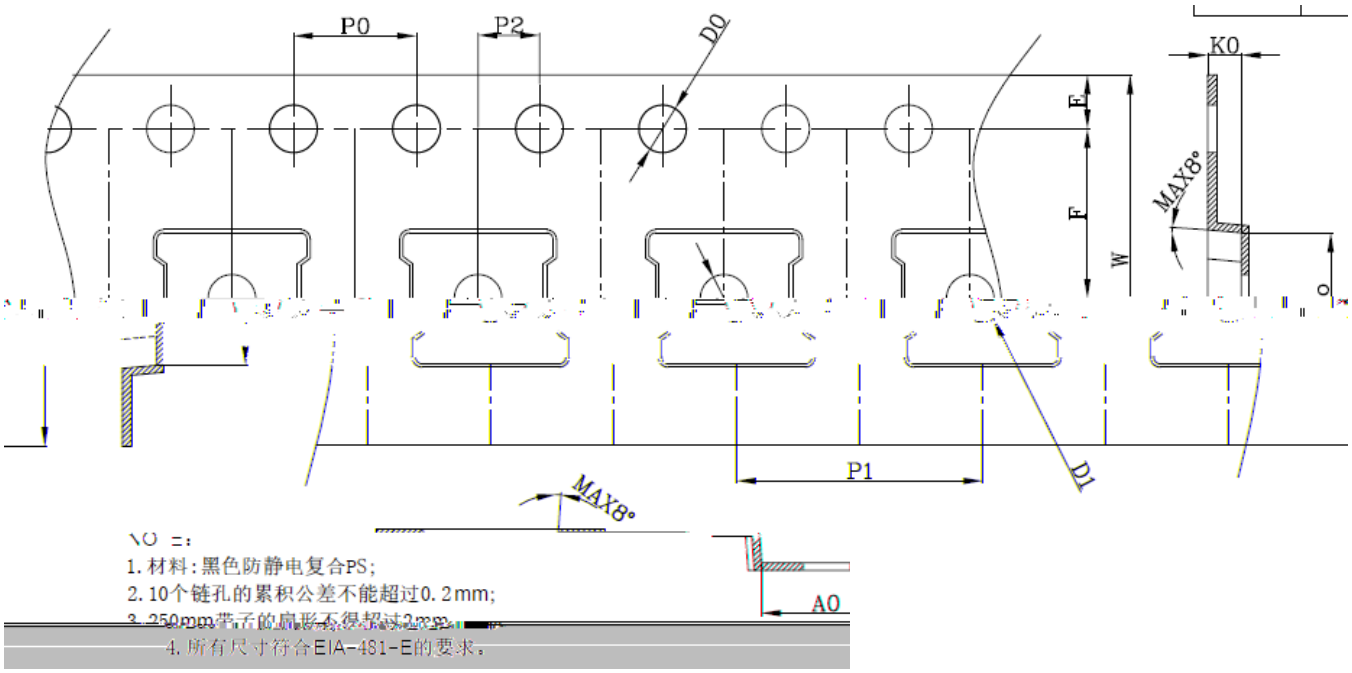
 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS				
TYPE WIDTH	∅A	∅N	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved



1. 材料：黑色防静电复合PS；
2. 10个链孔的累积公差不能超过0.2mm；
3. 250mm带子的扇形不得超过2mm。
4. 所有尺寸符合EIA-481-E的要求。

SYMBOL	A0	B0	K0	P0	P1	P2
0.10	8.00±0.10	2.00±0.05	SPEC	4.30±0.10	4.30±0.10	1.10±0.10	4.00±

)	D1	W	SYMBOL	T	E	F	D(
0.05	1.55±0.10	12.00±0.30	SPEC	0.30±0.05	1.75±0.10	5.50±0.05	1.55±

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved