

SCT71801A00 Series

REVISION HISTORY

127(3DJH EH I H L H L L D QJH I DJH EH L KHF H H L
5H L L 5HHD H G F L .

DEVICE ORDER INFORMATION

Orderable Device		Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
6&7	07(5	G	(0 6 2 3 /				7D H 5HH

PIN CONFIGURATION

RECOMMENDED OPERATING CONDITIONS

2 H HDLJ I H HDL H HD H D JH H KH LH HG

PARAMETER	DEFINITION	MIN	MAX	UNIT
9 ₁	, DJH D JH			9
9 ₂₈₇	2 DJH D JH			9
9 ₍₁	(DEHL DJH		9 ₁	9
9 ₃	3 H J G L DJH			9
(/ <	3 J D DEH3 H G HD 7L H			9
& ₁	, FD DFL			)
& ₂₈₇	2 FD DFL			)
(65	2 FD DFL (65 H LH H			
7-	2 HDLJ FL H HD H			&

ABSOLUTE MAXIMUM RATINGS

2 H HDLJ I H HDL H HD H D JH H KH LH HG

PARAMETER	DEFINITION	MIN	MAX	UNIT
9 ₁	0 D L L DJH D JH			9
9 ₂₈₇	0 D L DJH D JH			9
9)%	0 D L I H G E D F L DJH			9
9 ₍₁	0 D L H DEHL DJH		9 ₁	9
9 ₃	0 D L H J G L DJH			9
9 ₃ /	0 D L H J G HD L DJH			9
7-	- FL H HD H D JH			&
7 J	6 DJH H HD H D JH			&

(1) 6 H H EH GK HLHG GH E H0DL 5DLJ D FD HGH IEH H DH G DJH 7KHG IEHL J DD HG
I FL IGH IL 5HF HGH2 HDL & GL

(2) F H L L HL K GEHF HFHGEH HH 3 D GK H HG H HJ 9287 KH H : KH KH HG
H L KJ KH KD 9 KH DL & H / L L L EH H H KD HF KH=H H

(3) 2 HDL LKL KL D JHD IG H DH GH IEH G DJH K JKHF IFD HI D FHL J DD HG IGH KH HDLJ
D EH H HD H D JH

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
9 ₍₆	+ D % G 0 GH + %0 H 16, -((& -6 H F I E D L D L			9
	& KD JHG H IEH 0 GH & 0 H 16, -((& -6 H F I E D L D L			9

(1) -((& GF H -(3 DH KD 9 + %0 D DH D IDF LJ LKD D G(6 F FH
(2) -((& GF H -(3 DH KD 9 & 0 D DH D IDF LJ LKD D G(6 F FH

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ELECTRICAL CHARACTERISTICS

9,1 9287 9 &287) 7- & & IED D HL H HG GH &

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
9,1	2 HDLJL DJH					9
9 _{89/2}	9,1 89/2 7KH K G + HHL	9,1 LLJ				9 9
,6+ 1	6K G F H I 9,1 L	(1 9,1 9				
		(1 9,1 9				
,4	4 IH FH F H I 1 L	(1 I D DG 9,1 9 7- &				
		(1 I D DG 9,1 9 7- &				
		(1 I D DG 9,1 9 7- &				
		(1 I D DG 9,1 9 7- &				

Regulated Output Voltage and Current

9)%	)HGEDF DJH DFF DF	7- &				9
		7- & &				9
9 ₂₈₇	/LH HJ DL	9,1 9 ₂₈₇ 9 9				9
	/ DG HJ DL	,				9
9 ₅₂₃	DJH	9,1 9 ₂₈₇ 9 ,				9
		9,1 9 ₂₈₇ 9 ,				9
,287	2 F H	9 ₂₈₇ L HJ DL				
,2&	2 F H L L					
,2&)%	2 H & H) GEDF	9,1 9,1B+, + 9				
3655	3 H HHFL DL	9 ₂₈₇ 9 , I + &287)				G%
		9 ₂₈₇ 9 , I + &287)				G%
		9 ₂₈₇ 9 , I + &287)				G%

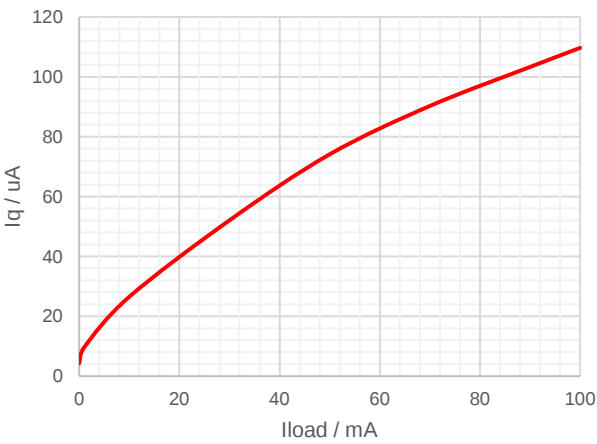
Enable and Soft-startup

9(1B+	(DEHKJK KH K G					9
9(1B/	(DEH KH K G					9
9(1B+	(DEH KH K GK HHL					9
,(1B 9	(DEH L F H	(1 9				
766	6 I D L H					

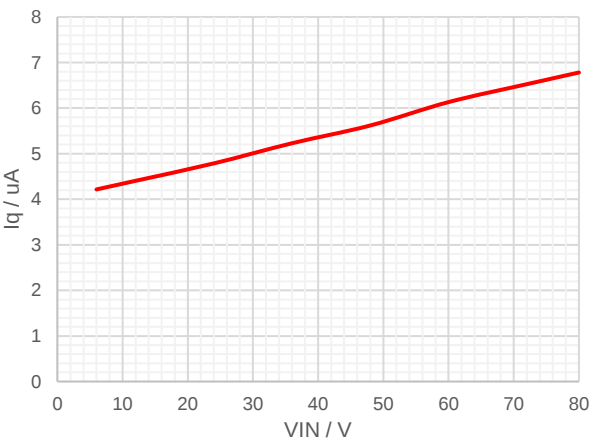
Power Good

9 ₃ B5	3 LLJ KH K G HFH DJH	9 ₂₈₇ 9 ₂₈₇ 120 KH 9 ₂₈₇ LLJ				
9 ₃ B)	3 ID LJ KH K G HFH DJH	9 ₂₈₇ 9 ₂₈₇ 120 KH 9 ₂₈₇ ID LJ				
9+<6	3 L K HHL					
9 ₃ B/2:	3 DJH	VOUT=0.8XVOUT(NOM),PG sink 100uA		76		9

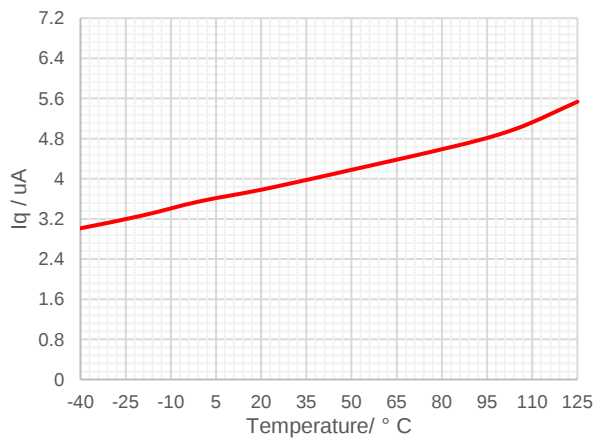
TYPICAL CHARACTERISTICS



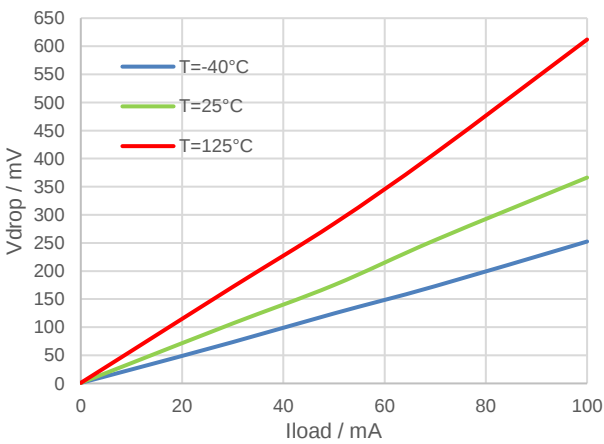
) U H 4 IH FH & H 2 & H



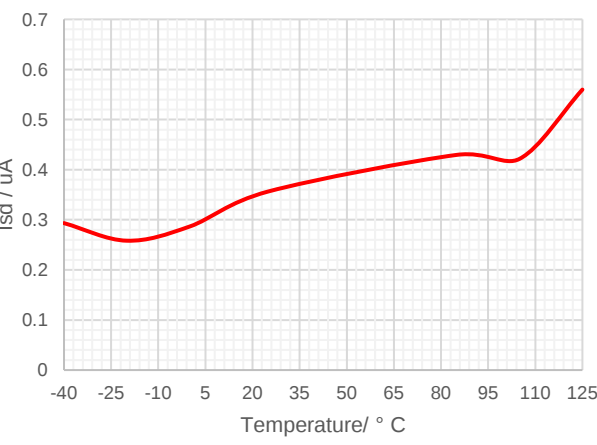
) U H 4 IH FH & H , 9 DJH 1 DG



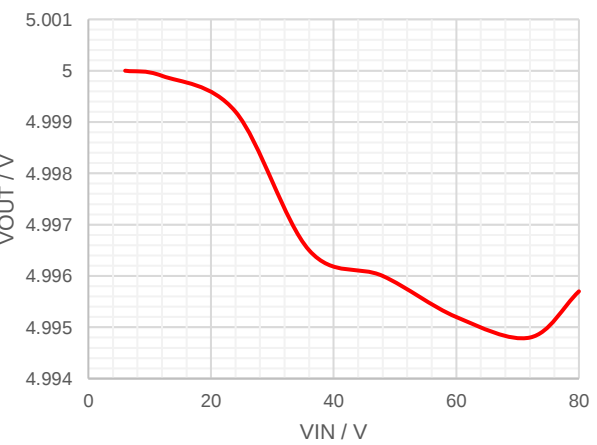
) U H 4 IH FH & H EIH 7H HD H



) U H 9 DJH 2 & H

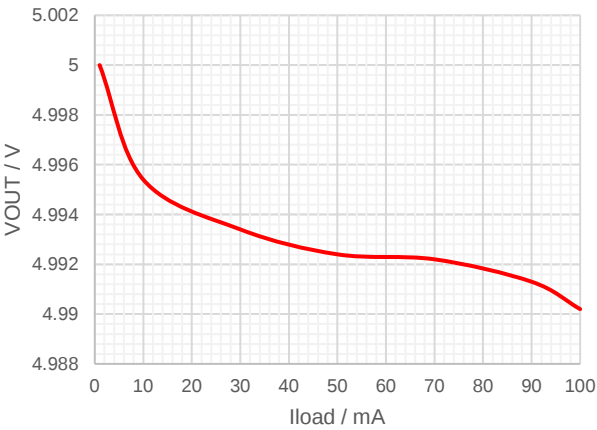


) U H 6K G & H EIH 7H HD H

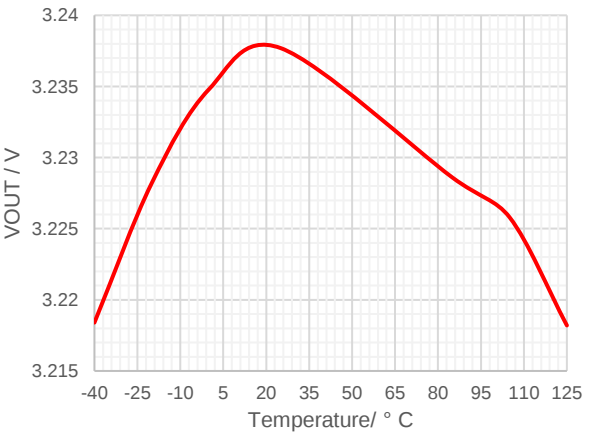


) U H 2 9 DJH , 9 DJH

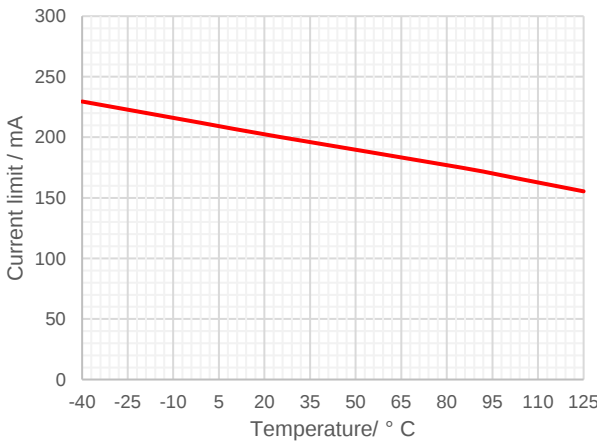
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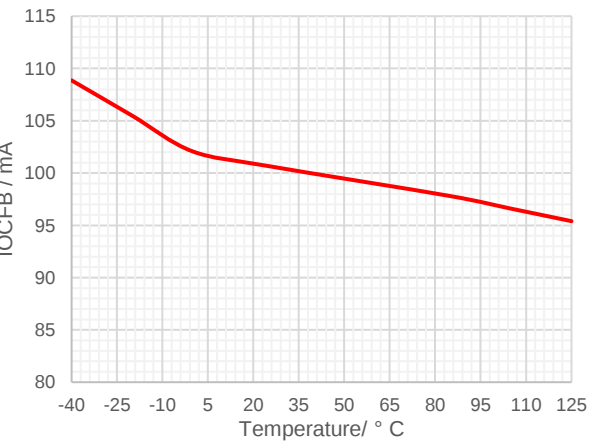
) W H 2 9 DJH 2 & H



) W H 2 9 DJH 9 287 9 EH 7H HD HD



) W H 2 & H / L L 9 9,1 9 EH 7H HD HD



) W H 2 & H / L L 9 9,1 9 EH 7H HD HD



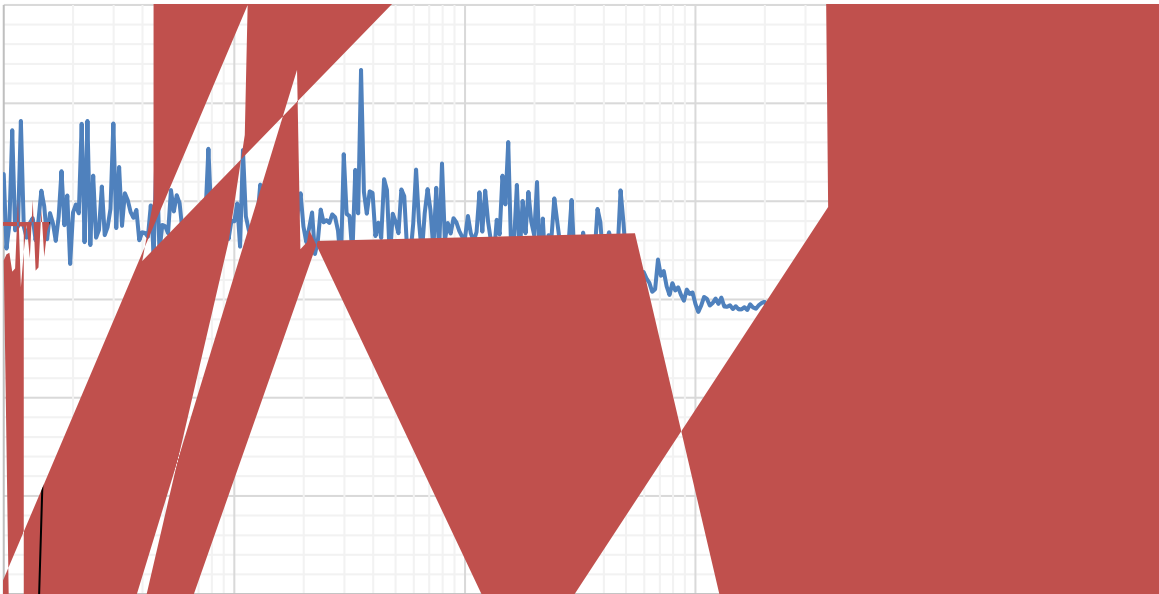
TYPICAL CHARACTERISTICS (continued)



9287)W H 3655) H H F
9 &l) &287) ,287

9,1)W H 3655) H H F
99287 9 &l) ,287

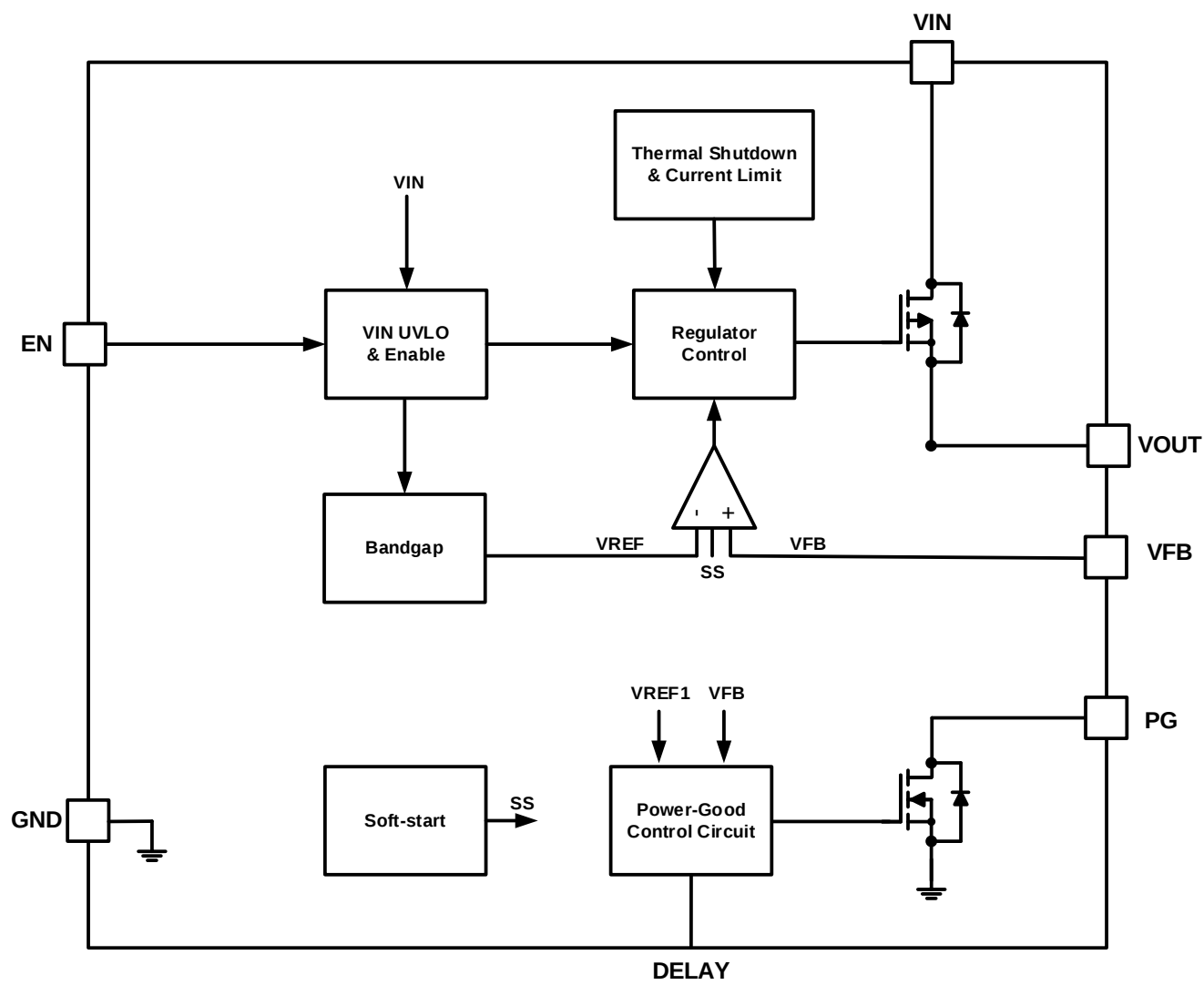
TYPICAL CHARACTERISTICS (continued)



)W H 3655) H H F
9,1 9 &l) &287) ,287

)W H 3655) H H F
9,1 9 9287 9 &l) &287)

FUNCTIONAL BLOCK DIAGRAM



) W H) F L D % F I D J D I G 2 9 H L

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OPERATION

Overview

7KH6&7 H I H G F D H I G H L D J H D J H L H D H J D L K H I H F H
 F H 7KH H D J H H J D H D H I 9 9 & L D J H D G F H I H F H F H D
 D G

7KH6&7 H I H G F L D E H L K)) F D D F L D G) F H D I E F D D F L L
 H F H G H G L H D I D L H D I G D J H L K F H D G D J H H K G L J
 D

7KH6&7 H I H G F D I G H H D E H F 3 H G I H D H D G J D D E H 3 H
 G G H D L H K I F K L H L D E H I K H D I E D L H H G L J H H F H F I W D L 2 K H H F L
 I H D H L F G H K H 9,1 L G H D J H F H F H H F L K D G K H F L D G
 K H D K G H F L

7KH6&7 H I H G F I G H D G D E H H L I 9 9 J H H G D H
 D J H H L D H D F D J H L H D H I H H I H F D F 6&7 D H

Enable and Under Voltage Lockout Threshold

7KH6&7 H I H G F L H D E H G K H K H 9,1 L D J H L H D E H 9 D G K H (1 L D J H
 H F H G K H H D E H K H K G 9 (1B+ 7KH G H I E H L G L D E H G K H K H 9,1 L D J H I D E H 9 K H K H
 (1 L D J H L E H 9 (1B/ , H D F H F H (1 L D K H G H I E H H D E H K H (1 L I D
) D K J K H H 89/2 K H K G F H F D H H D H L G L I G H 5 D G 5 I 9,1 1 K L
) W H 7KH 89/2 L L J D G I D L J K H K G F D E H F D F D H G E (D L D G (D L H H F L H

: K H H

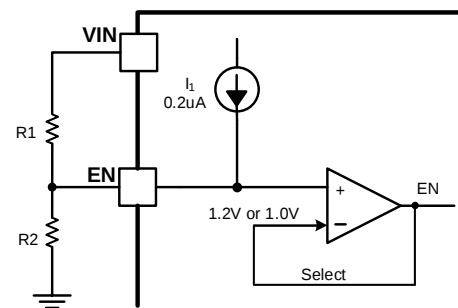
9,1 L H 9 L L H K H K G H D E H K H G H I E H

9,1 K 9 L K H H L K H K G

, D G F G E H H J H F H G L K H F D F D L

9 (1B+ 9

9 (1B/ 9

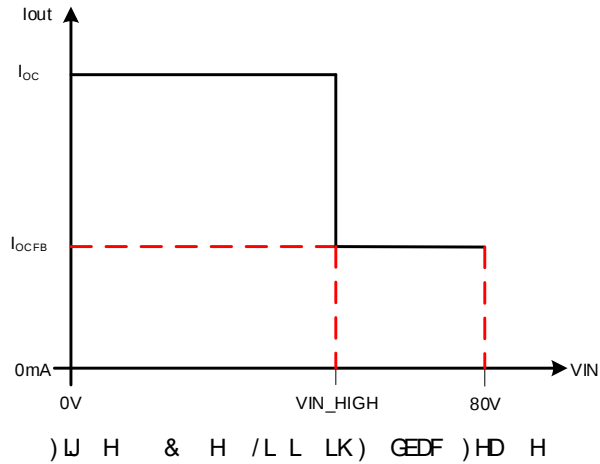


) W H 6 H 89/2 E H D E H G L I G H

Regulated Output Voltage

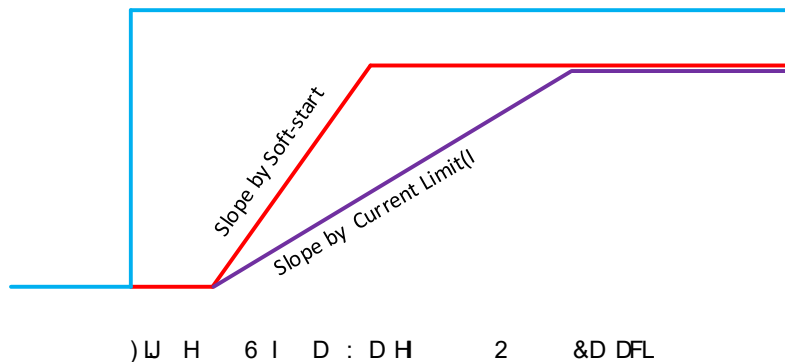
: K H K H L D J H L K J K H K D 9 287 120 9 523 L L K H H J D H G E D H G K H H L H G
 D J H H L : K H K H L D J H I D E H 9 287 120 9 523 L D F K H L D J H L K H
 G D J H E D H G K H D G F H : K H K H L D J H G E H 89/2 K H K G K H H H
 G H D H G 2 7 K H K G

7KH DJHL HJ DHG KH KHGH IEL L L F H L L : KH DF H L L H H FF KH
HJ D EHJL KHD EHF D H I KHL FHD HL HGL LDL ,I KH D K G L WJH HG KHGH IEL
II IH KHGH IEL F G KHL H D KH D K G FLF L KHGH IEL EDF ,I KH
F H ID F GL H L KHGH IEL F H EH H F H L LD G KH D K G
: LK KH H F H VIN_HIGH Control IHD H KH 6&7 H IH GF GEH H E D G
DH KH H F H ID D G K LJH H FF % LD H LH KH DL DGL J F H K G
EH DH KD ,2&)% G LJ D 7KH FK D F HL IEL K L KHI LJ I H



Internal Soft-Start

7KH 6&7 H IH GF L HJ DH D L H D I D FLF L KD D KH H H H FH DJHI
H 9 H H H FH DJHL ,I KH (1 L L HGEH 9 / 2 L EH K IID G KHL H D
I D H H 7KH I D D H H G LJ K G GH KH D H DGL J
% H I W H K KH D DH D D FD DFL D G DJH FD DFL : KH
FD DFL L D I HD H) KH H I 9287 L L L E I D : KH FD DFL L DJH I
HD H) KH H I 9287 L L LHGE F H L L ,2& D 9,1 VIN_HIGH D G KH H I 9287 L
L LHGE F H L L ,2&)% KH 9,1 VIN_HIGH
, 6&7 H IH GF IED 7 L D G IED ,2& L D G IED ,2&)% L F G
H KHI LJ I DI L L ID D L HFDF DL



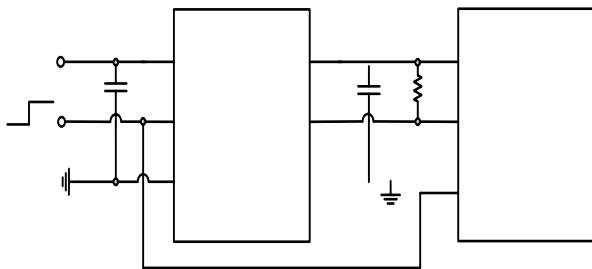
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Power-Good and Power-Good Delay

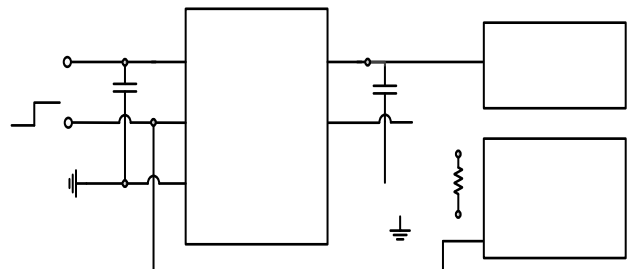
7KH H J G 3 L L D H GDL D GFD EHF HFHG D 9 H DL K JKD H H D
 HL 7KH3 L KJL L HGD FH KH 9287 L JHDH KD KH3 L KH K G 9₃ B5
 9_{287 120} ,I9287 G EH 9₃ B) 9_{287 120} KH H GDL D G KH3
 ,I DJH L L J L HHG KH3 L FD EH H I DL J F HFHG 1

,I KH H J GGD L HL H JKI HD IEDL F GF HF DH H D FD DFL I (/ <
 L 1 KL FD DFL L FKDJHG 9 9 E KH (/ < L F H , (/ < D GJH HDHH DGD
 L H. When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}.
 The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when C_{DELAY} =
 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.2V) / 1 μA = 12 ms.

7 H H H HDL I KH H J GIHD H DL DL 9,1 9 9,1B0,1 , D F HFL I 3
 L FLF L LK KH D H GUHH H DJH KH / 2 9287 H H %H DH KH F HFL
 HD H



)U H 3 & HFHG / 2 2



)U H 3 & HFHG KH KH 3 H 6

%H IU H K KH D D G K G L DL KH H D G H G
 KH L KHL DJH D LHI 9 / 2 L L K G HFD H9,1 L EH L 89/2
 KH K G D G DJHL 9

KH L KH9,1 DJH HFDKH 89/2 KH K G H H D G / 2 D FKDJLJ I FD DFL 9287
 LLJ HGL GHLHGE L H D I D I FL

KH L KH9287 DJH HFDKH D KH9,1 DJHD L LH ID H D G / 2 JH L G HJL
 7KHGUHH FHEH HH 9,1 D G9287 L KHG DJH

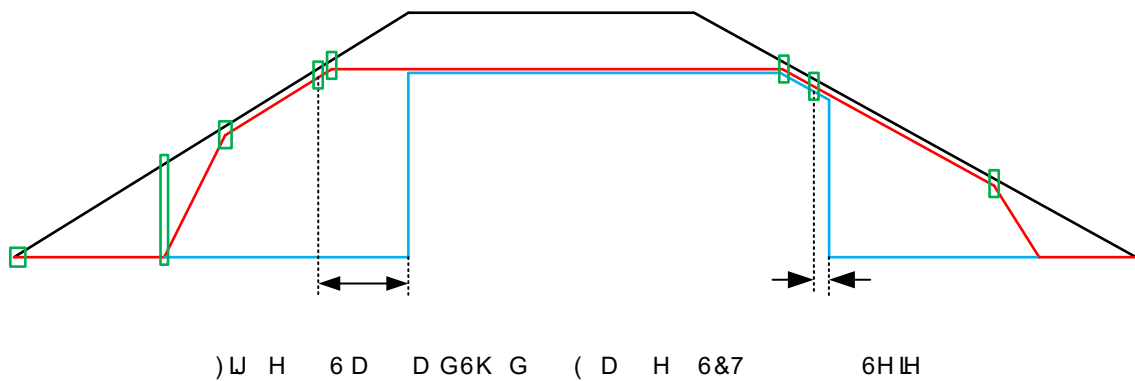
KH L KH9287 HFDKH 3 KH K G 9₃ B5 9_{287 120} D GI KL L / 2 F KH H
 J GGD L H I H KL GHD KH3 L LH KJLKH H K LJ KD 9287 L

KH L KH9287 HFDKH L LD D H 9 H L D KH9,1 D EHKLKH KD 9_{287 120}
 9 523 D G / 2 JH L HJ DL HJL

KH L D KH9,1 DJH H G D G / 2 H G HJL DJDL

KH L KH9287 G EH 3 KH K G 9₃ B) 9_{287 120} D G / 2 D F LJ KH H
 J GGU LFK L H KFKILH ID 9287 GH K FD HGI HD HE LH DG D IH H H IH
 KL GHD KH3 L K HG 9 H H KJLKH HIDL DH

KH L KH9,1 DJHL H KD L DJH89/2 KH K G L 89/2 K HHL HHD G / 2
 J H L KH K G DH



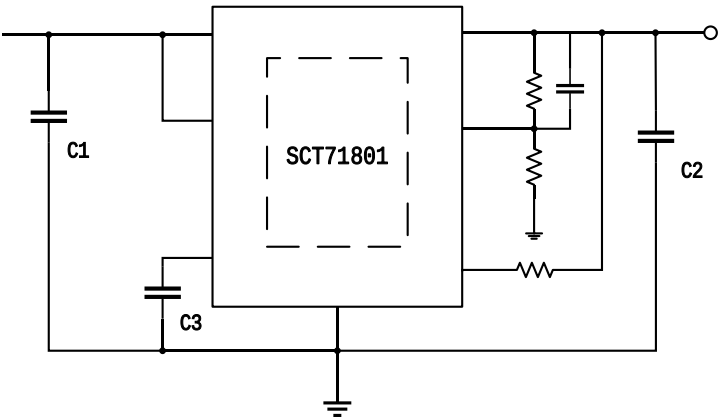
Thermal Shutdown

7KL GH IEHLF DH D KH D K G 7₆ FLF LD D HFL I HKDLJ) F L D
HDL KH FL H HD H K G H FHG KH7₆ L L 7KH FL H HD HH FHGLJ KH
7₆ L L FD H KH II : G D H HD 0DK7K G

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APPLICATION INFORMATION

Typical application 1:

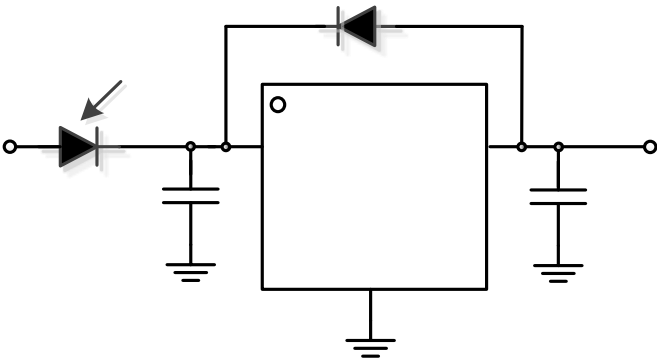


)W H 6&7 7 IED IEDL 6FKH DIF

Design Parameters

Design Parameters	Example Value
, 9 DJH	9 1 D 9 9
2 9 DJH	9 9 9
0 D L 2 & H	
2 &D DFL 5D JH &	)) HF H G)
, &D DFL 5D JH &	) HF H G)
3 H L I H J G 5	

Typical application 2:



)W H 6&7 7 IED IEDL 6FKH DIF LK5H H H3 DL LGH

Design Parameters	
Design Parameters	Example Value
, 9 DJH	9 1 D 9 9
2 9 DJH	9 9 9
0 D L 2 & H	

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Output Voltage

7KH DJHL H E D H H D H L GLIGH 5 D G5 L IED D IED L FKH DIE 5HF H GHG
5 H L D FHL 8 HH DL FDF DH5

KHH

9₅() L KHHHGEDF HHH FH DJH IED 9

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

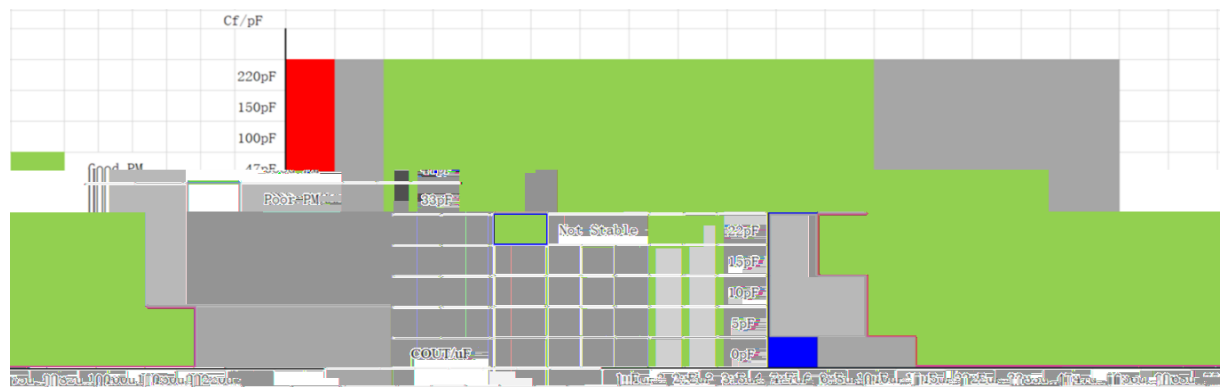
9 9	&287)	&l)	5	5	&287) (65 L D

Input Capacitor and Output Capacitor

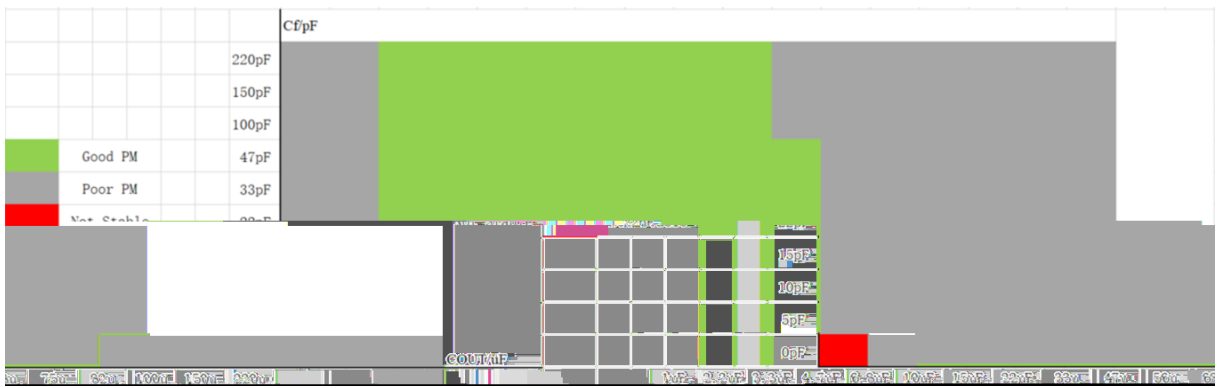
6&7 HF H G DGGJ D) J HDH FD DFL LKD) E D FD DFL L DDH D 9,1 L HH
KHL DJH DEH L HHF IED DFL KH FD DFL LK KWKFD DFLD FHL JJH HGI
KH H H LK DJH DJH LH 7KH DJH DLJ I KHFD DFL EHJ HDH KD KH D L
L DJH

7 H H DELL KH 6&7 GF H LH D FD DFL LK D LL HHFLH
FD DFLD FH D H I) GKH G F F G FD DFL D JHI)) D G LK
D (65 D JH EH HH DG 6&7 HF H G HHFLJD; 5 ; 5 H)) FHD IE
FD DFL LK (65 H H HD H DJH L H KH DG D IH H H

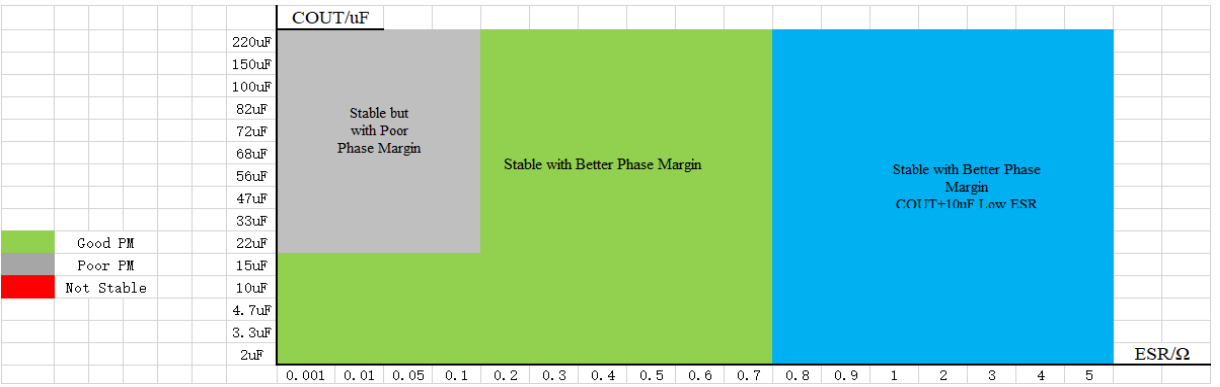
: KH LJ DJH FD DFL LK KWKH (65 H L I HD H) HHF IED DFL LK
(65 H L L KHD IEDL 6&7 HF H G DGGJ J H D) (65 FD DFL DDH
F HFL LK KH DJH HHF IED DFL KL LHL LDH KH GH K H K DJHFD HGE KH
DJH(65 H L D GJH EH H DG D IH HI D FH



) W H 6 & 7) H G) D G & D D F L H F H G 5 9 2 8 7 9



) W H 6 & 7) H G) D G & D D F L H F H G 5 9 2 8 7 9



) W H 6 & 7 6 D E L L 9 6 2 & D D F L

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Power Dissipation and Thermal Performance

3 H GL LDL FD HGE DJHG DF KH / 2 DGE KH F H I LJ K JK KHGH IEH
 HHG EHGL LDHG I KHFKL 7KH DL FL H HD HL GH GH H GL LDL
 DF DJH KH3&%D EH I HG& DH & DH KIE H D GKHD EIH H HD H

LJ D HDL / 2 FL H HD H K G H FHGH & H HL D H L GHHL DL
 I KH H IH I KHFKL 8 LJ EH H DL FDF DH KH H GL LDL D GH L DH KH FL
 H HD H

7KH H GL LDL FD EHFDF DHG LJ(DL %FD H, 1 ,287 KHH 9,1 , 1 L(DL F G
 EHL HG

7KH FL H HD HFD EHH L DHG LJ(DL 5 - B(90 L KH FL D EIH KH D H L D FH
 ED HG F H 3&%9HIL KHD IEDL D GD IIEIH DJL L KH KH D GH W E KHI LJ
 HK GL HG FDF DH KH FL H HD H7.

5 - B(90 L DF LIFD DD HH D GGH H G D IDF FKD KHI LJ

3 H GL LDL

L H HD HI

3&%DHD

& H KHD L DHD

1 EH I KH D ID GH KH DF DJH

GDFH F H DFH H

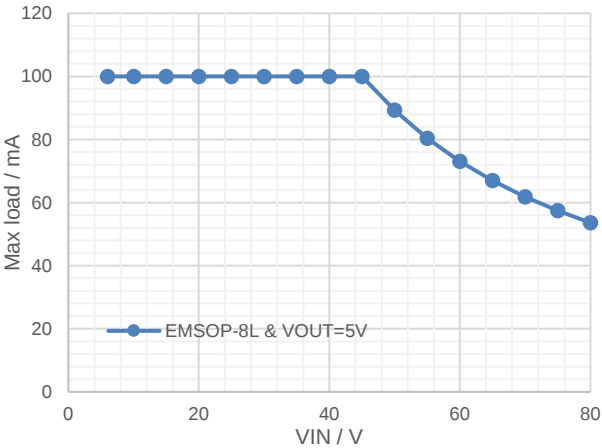
) KH6&7 GF KH DL D DEH H GL LDL I GH H DF DJH D L HGL KH
 I LJ DEH D G KH H H DHED HG (90 EDG DJH H GL LDL L WJH KH D
 K G HFL DH HF GFDF DH KH5 - B(90 I GH H DF DJH 7KHI LJ DEHL
 I HHH FHED HG (90 H HD H HD HH JK DJL KH GH W KH D HI DFH

7KH3&%LI DL I (90 DH & L H & LH

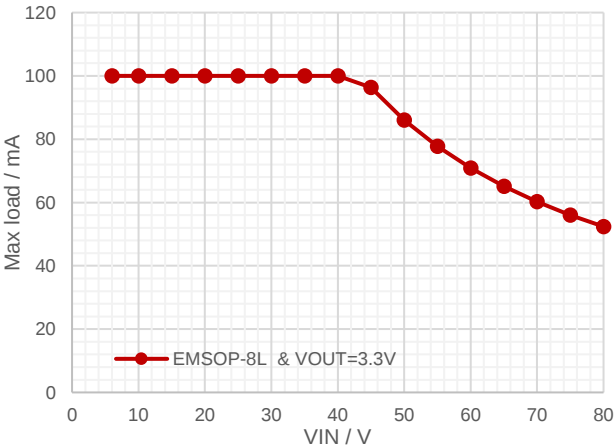
Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150)	R JA_EVM (°C/W)
(0623 /			

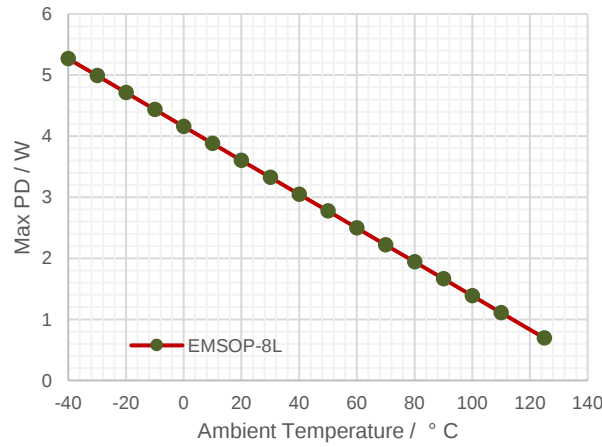
THERMAL CHARACTERISTICS



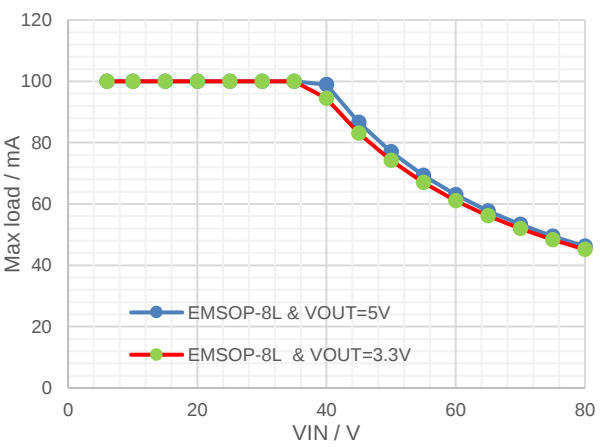
)W H 0D L 2 & H , 9 DJH
9287 9 I GWHH DF DJH 7. 76 B5



)W H 0D L 2 & H , 9 DJH
9287 9 I (0623 / 7. 76 B5



)W H 0D L HG3 H L LDL EIH
7H HD H (0623 / 7-

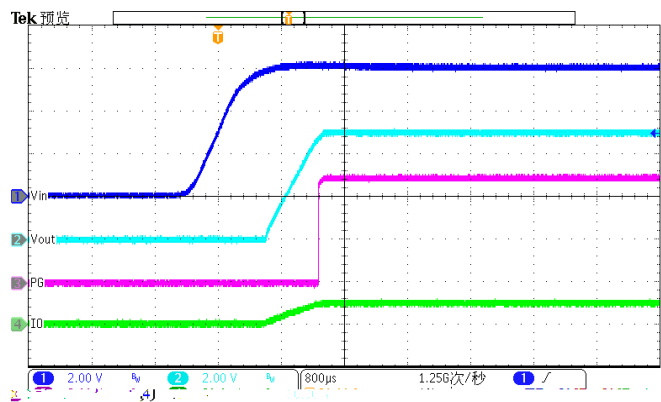


)W H 0D L 2 & H , 9 DJH
(0623 / 7-

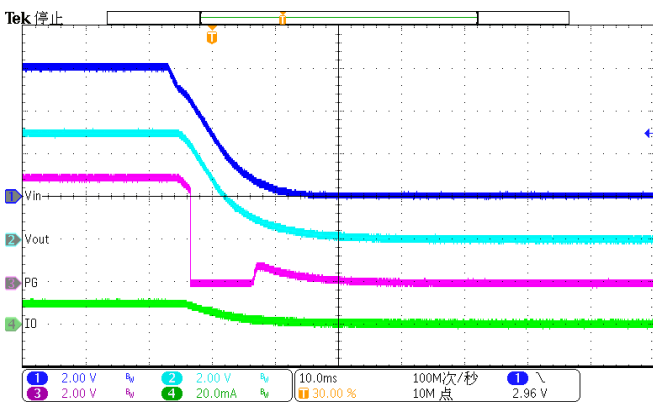
SCT71801A00 Series

Application Waveforms

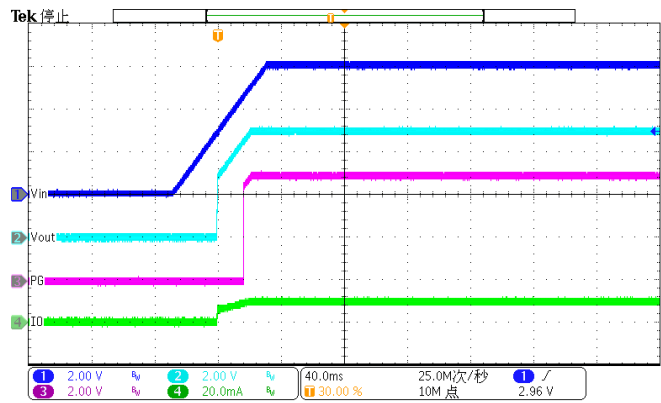
9L 9 9 H KH LH HG



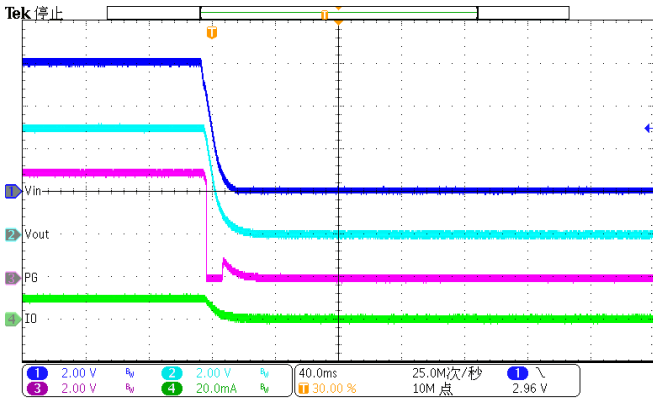
) W H 3 H , DG



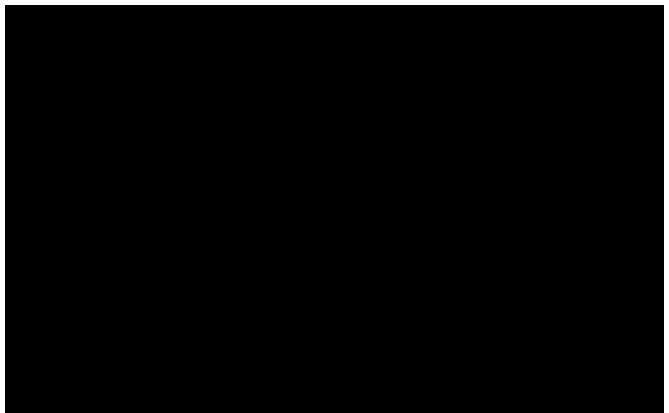
) W H 3 H G 3 L HG 9287



) W H 6 3 H , DG

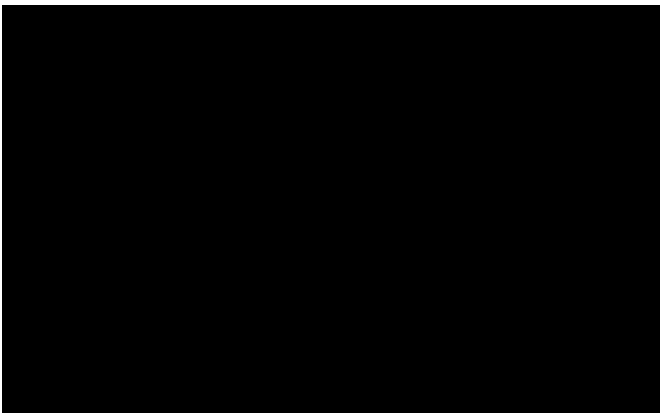


) W H .6 3 H G 3 L HG 9287



) W H & & / DG7 D IH

9287 9

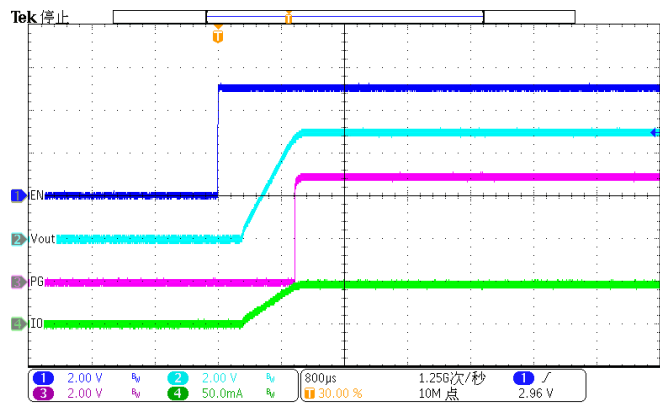


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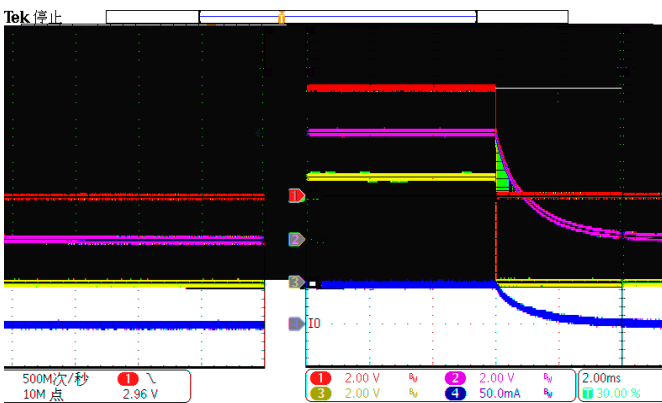
9287 9

Application Waveforms(Continued)

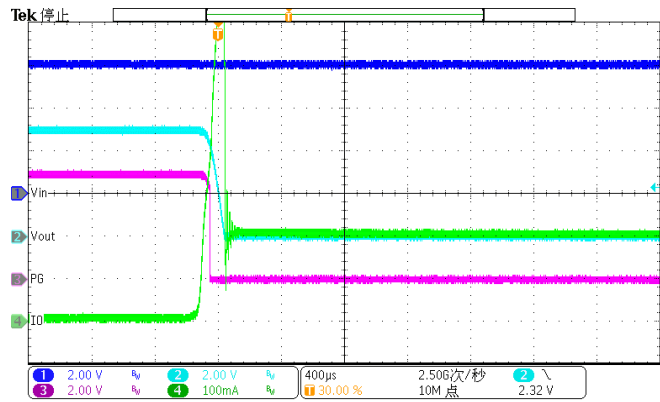
9L 9 9 H KH LH HG



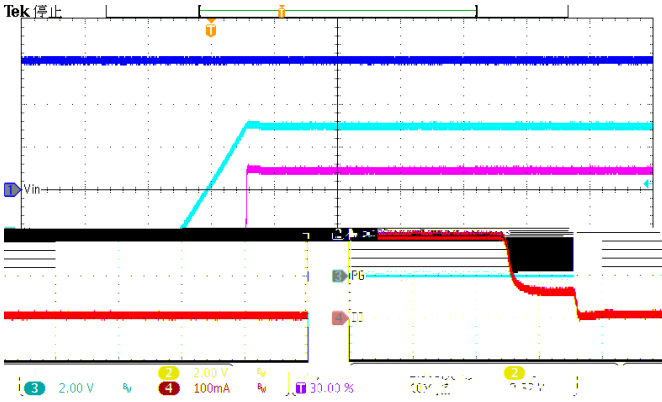
)W H (DEH , DG



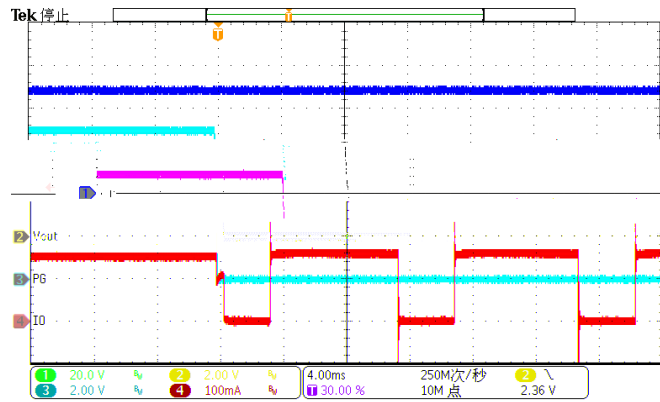
)W H LDEH , DG



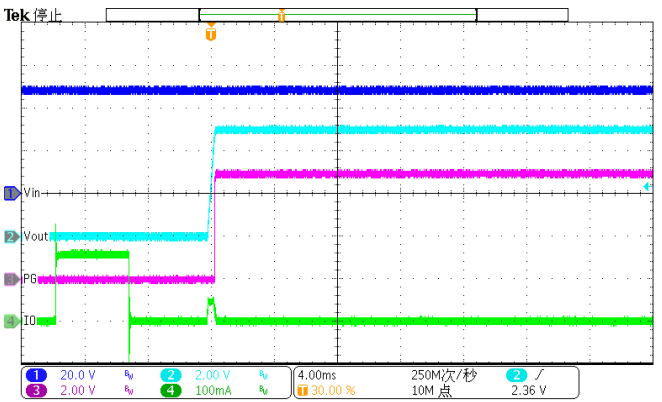
)W H (H 6K &LF L3 HFL



)W H .(L 6K &LF L3 HFL



)W H (H 2 H 7H HD H 3 HFL 9L 9

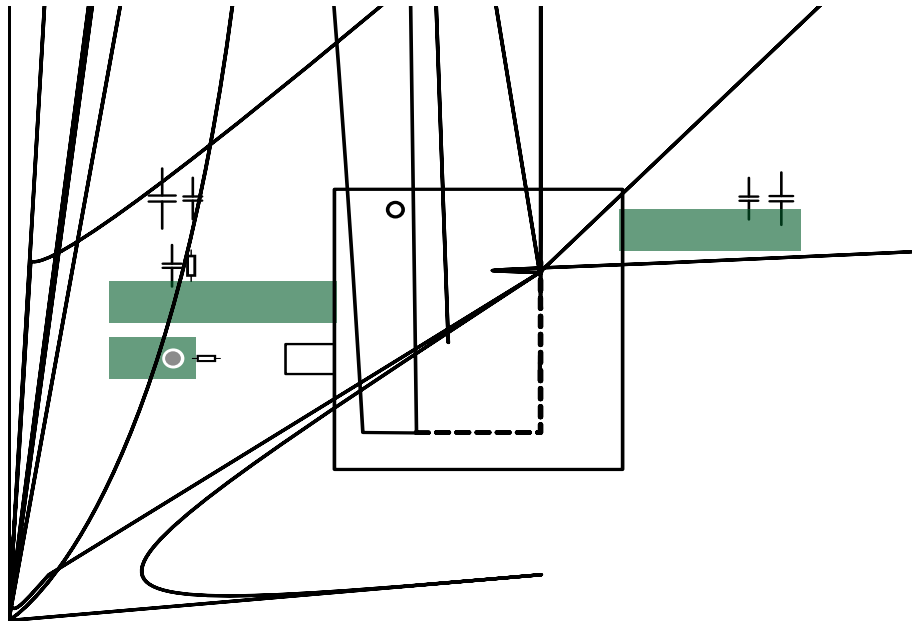


)W H (L 2 H 7H HD H 3 HFL 9L 9

SCT71801A00 Series

Layout Guideline

- 3 H 3&%D L DFLIFDI 6&7 DELL D IH HI DFHD GJ GHJ DL FKDDFHL IF
) EHH H I KH HJ IGH LH D EH
1. % KL FD DFL DG FD DFL EH DFHGD F H KHGH IEF L D IEH
2. , L HF H GHG E D KHL L J G LKD) E D FD DFL 7KH DHD I HGE
KHE D FD DFL F HFL 9,1 LDGKH 1 L I KH H EHD D D IEH
3. , L HF H GHG H IGH DFH H J K KIE F H HJ K L L LH, 5 G D GKHD GL LDL
4. 7 L H KH KH D HI DFH I KHGH IEF D G D L LH KH F H D KJ KD EIH H HD H
6&7 HF H G HDGL J KH F H GH KH KH D DGD ID D IEHD G DFL J H JK KH D
ID KH F H GH KH KH D DG
5. , I LJ DJHHHF IEF DFL LK KJ K (65 H L 6&7 HF H G DGGL J D) (65 FD DFL
DDHF HFL LK KH DJHHHF IEF DFL

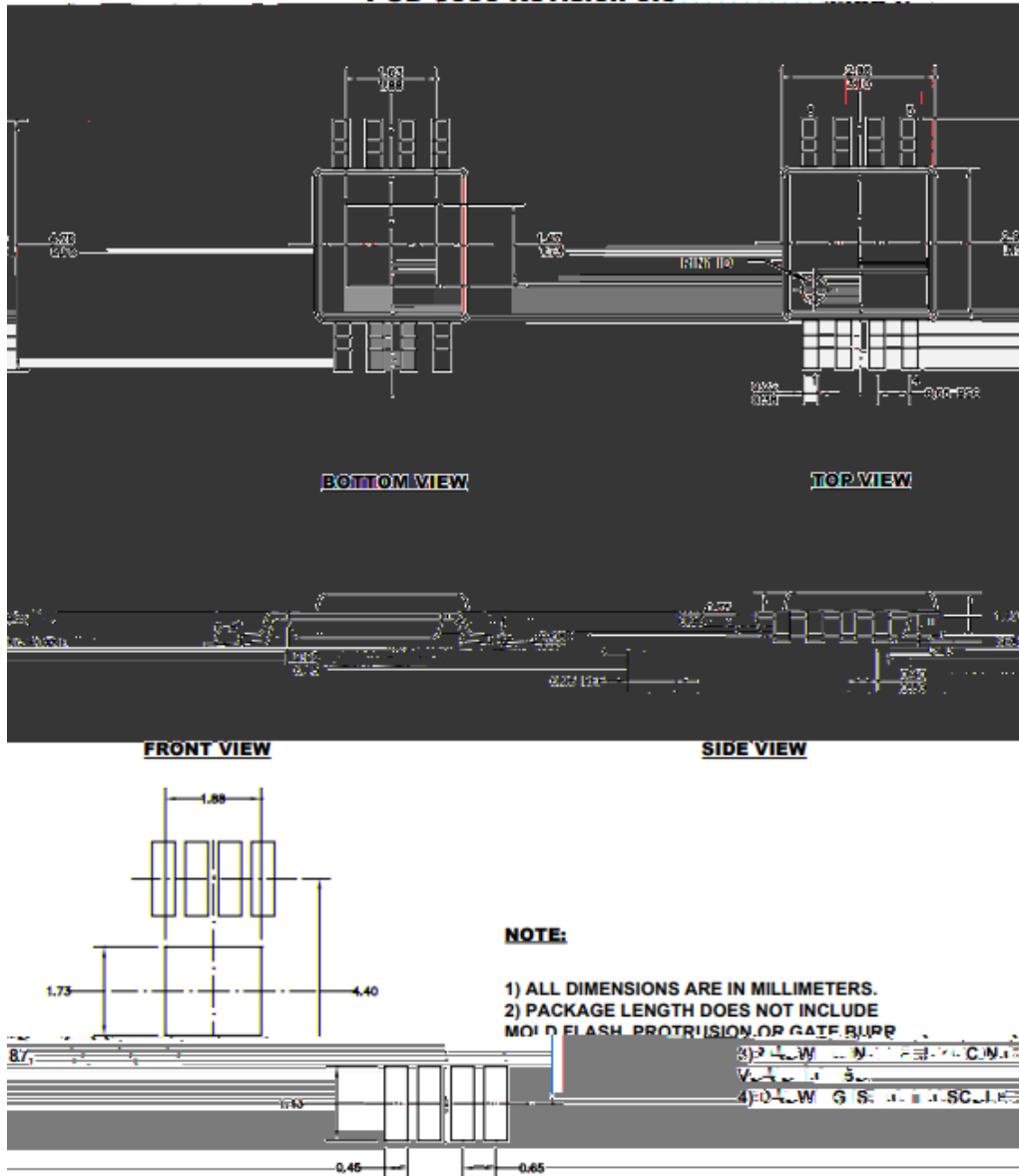


)W H 3&%/D (D H

SCT71801A00MTER

PACKAGE INFORMATION

PACKAGE OUTLINE DRAWING FOR MSOP8L-EP
POD-0050 Revision 0.0



RECOMMENDED LAND PATTERN

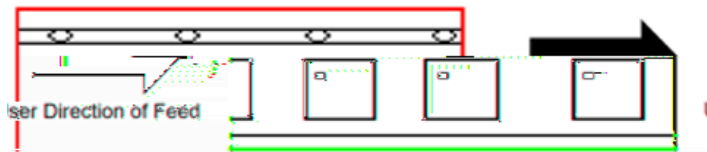
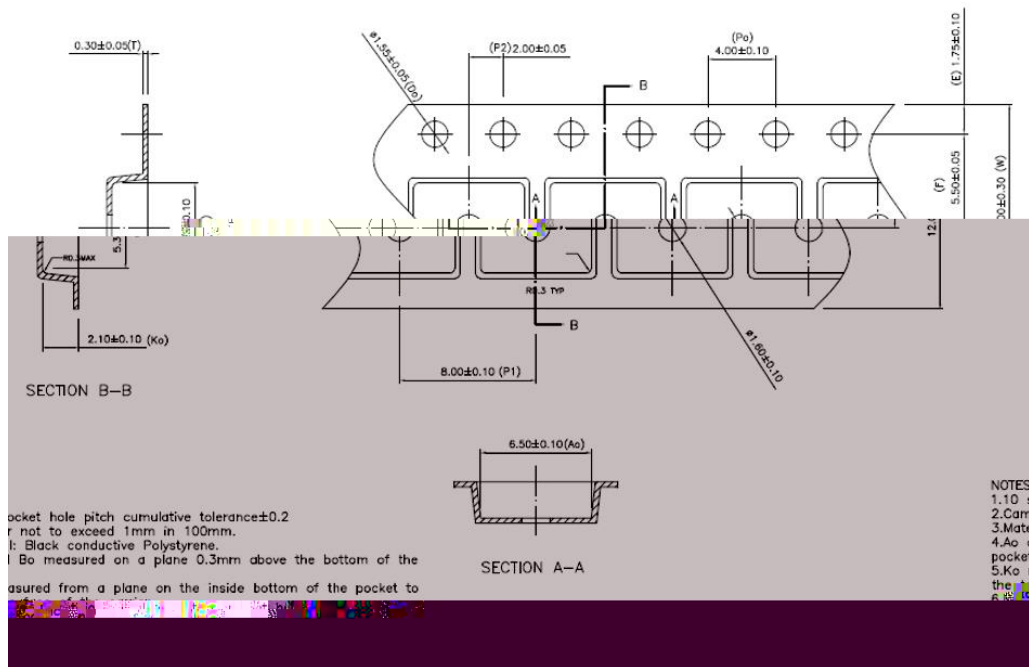
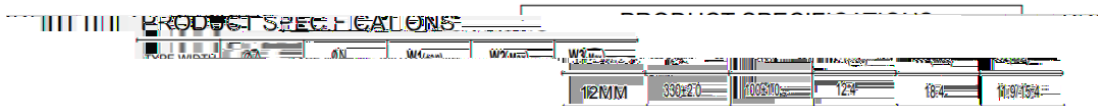
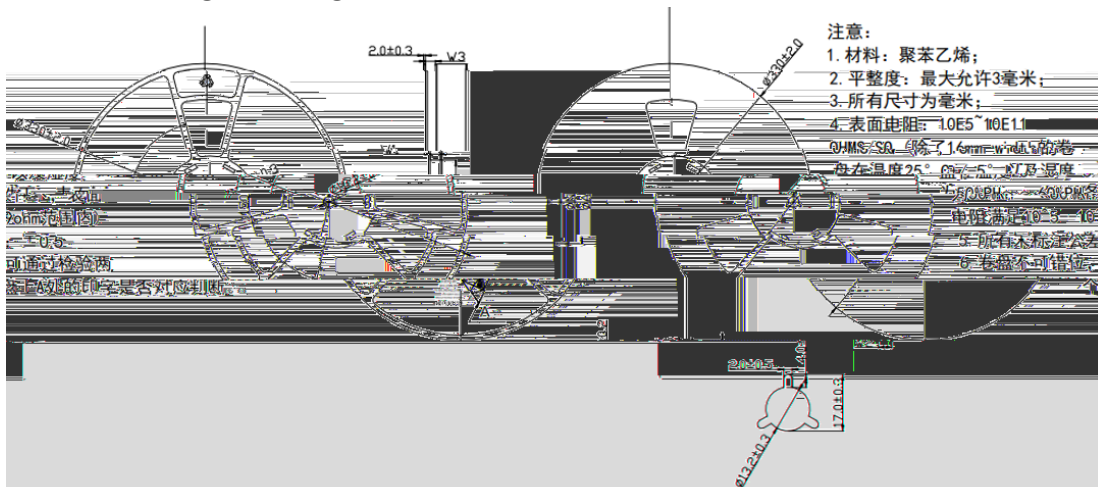
(0 6 2 3 / 3 D F D J H 2 L H L H L

NOTE:

1. D L J H G E H D G H D - (& D F D J H L H 0 2 D I D L
2. D L J F D H
3. L H D G L H L D H L L L H H
4. 7 K H D D G K D E H G H G K H E D G
5. L H L I H H G D G E I D F D J H G L F G H G I D K
6. & D F 3 % E D G I D E I F D L I L L G H D H E H D F H E H H K H L

SCT71801A00 Series

TAPE AND REEL INFORMATION



(0623 /

NOTICE: 7KHLI DL L KL GF H L EHF FKDJH LK IEFH 8 H K G D D DGJ DD HH KH KLG
 D , H H F D 3 H WK DH L L L JHG KH L H J D L J 6 L F & H 7 H F K J 6 & 7 G F L D
 D I F D L 6 & 7 L D HD H J D H I E L L I D D G D I F D L

) HLI DL L F H F 6 L F & H 7 H F K J & / G 5 W K 5 H H H G
 3 G F) G H / L 6 & 7 6 H I H

