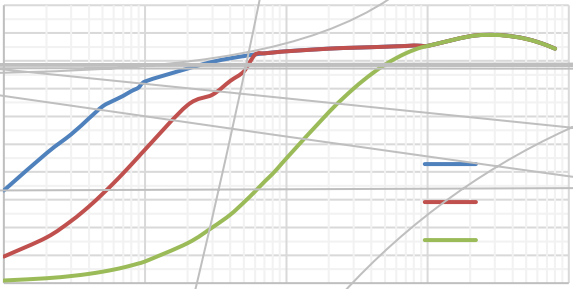
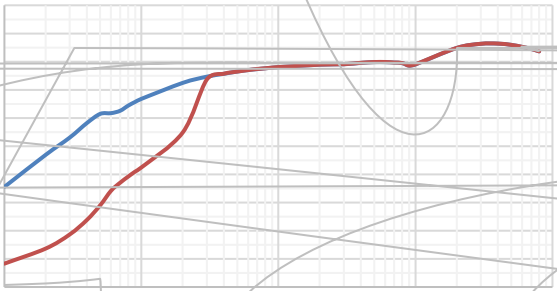
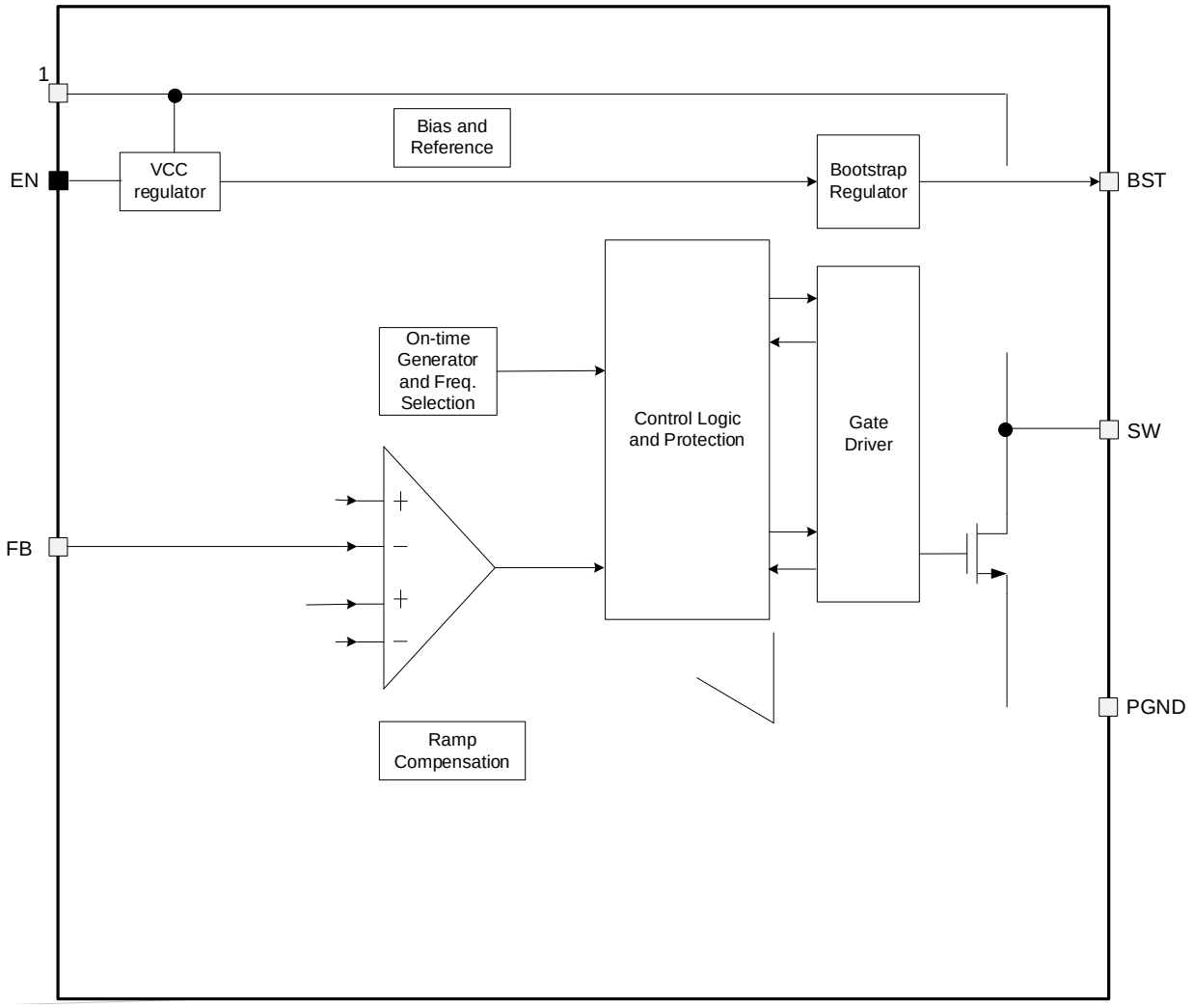
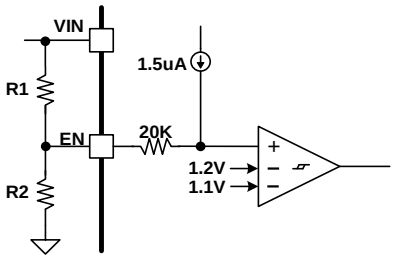





1
EN
VCC regulator
Bias and Reference
Bootstrap Regulator
BST
On-time Generator and Freq. Selection
Control Logic and Protection
Gate Driver
SW
FB
PGND
Ramp Compensation

Ω

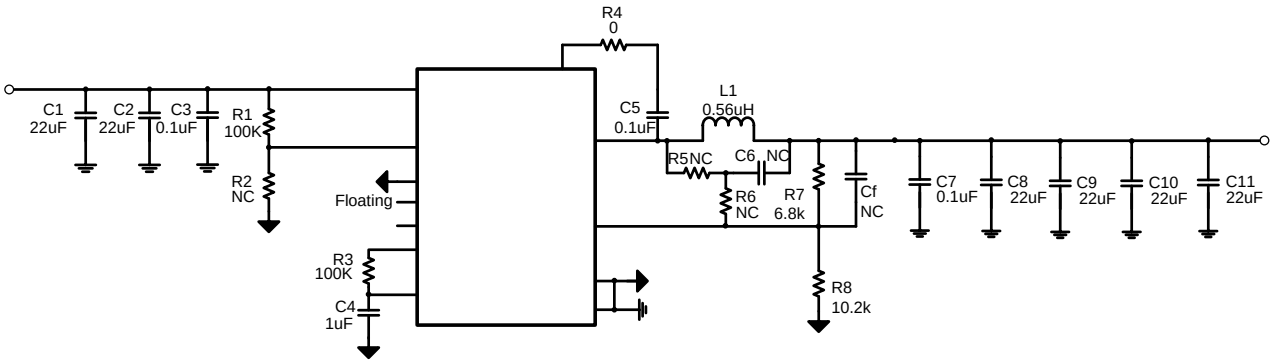
d

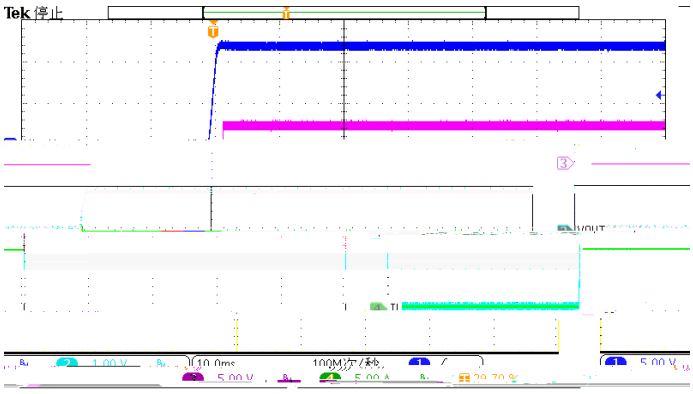


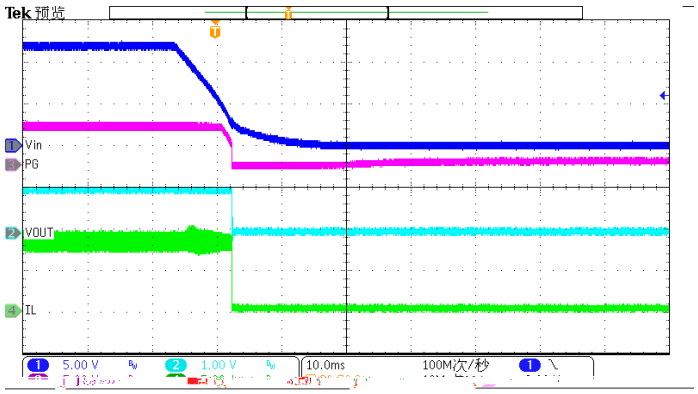
$$D \quad RMN \quad \frac{MSR}{PCD} \qquad D \quad MR$$

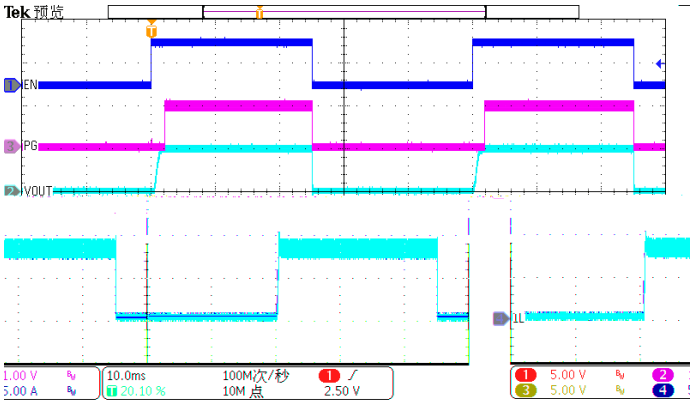
℃

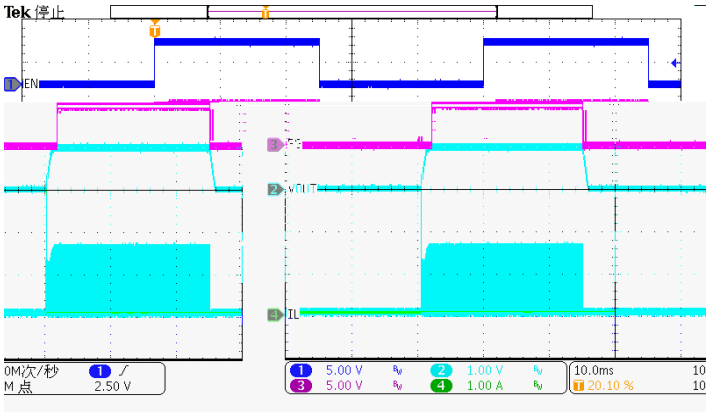
℃

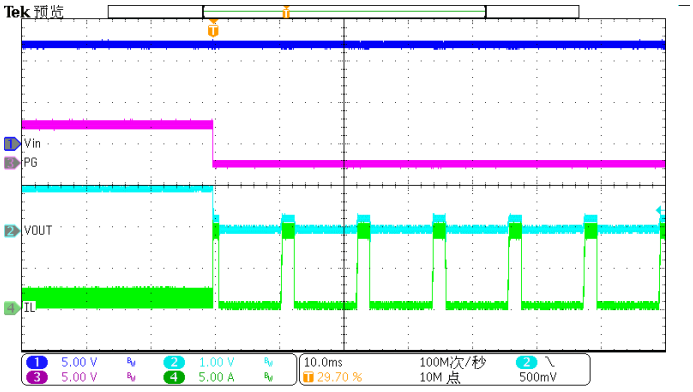

R4
0
C1
22uF
C2
22uF
C3
0.1uF
R1
100K
R2
NC
Floating
R3
100K
C4
1uF
C5
0.1uF
L1
0.56uH
R5NC
C6
NC
R6
NC
R7
6.8k
Cf
NC
R8
10.2k
C7
0.1uF
C8
22uF
C9
22uF
C10
22uF
C11
22uF

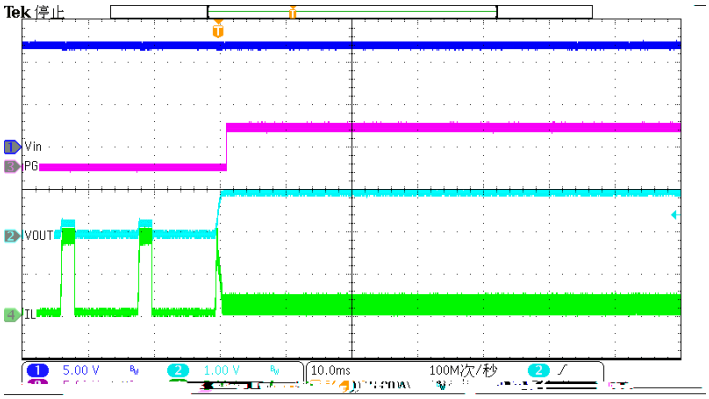

Tek 停止
VOUT
IL

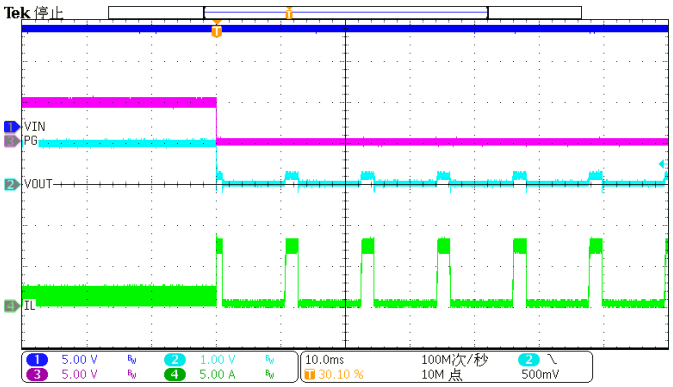

Tek 预览
Vin
PG
VOUT
IL
5.00 V
1.00 V
10.0ms
100M次/秒

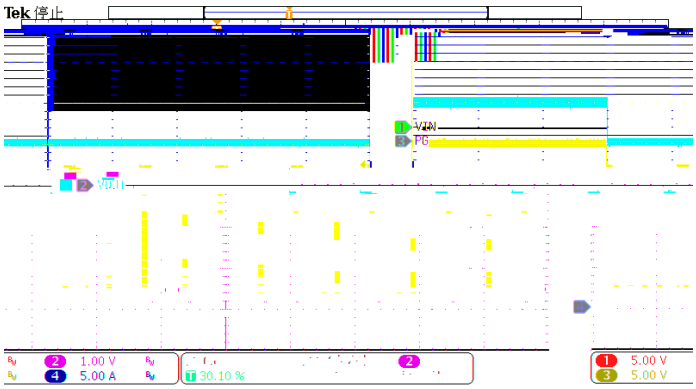

Tek 预览
EN
PG
VOUT
IL
10.0ms
20.10 %
100M次/秒
10M 点
2.50 V
5.00 V

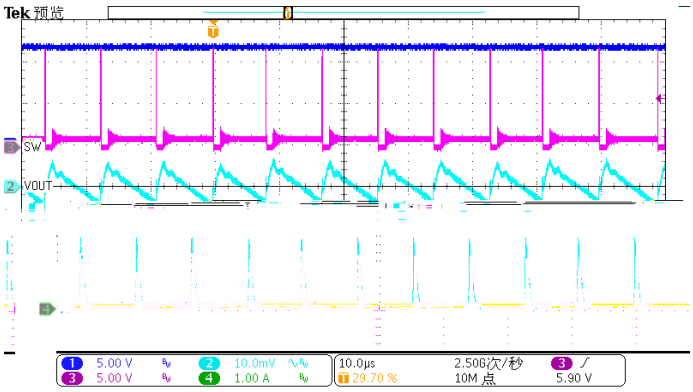

Tek 停止
EN
VOUT
IL
2.50 V
5.00 V
1.00 V
1.00 A
10.0ms
20.10 %

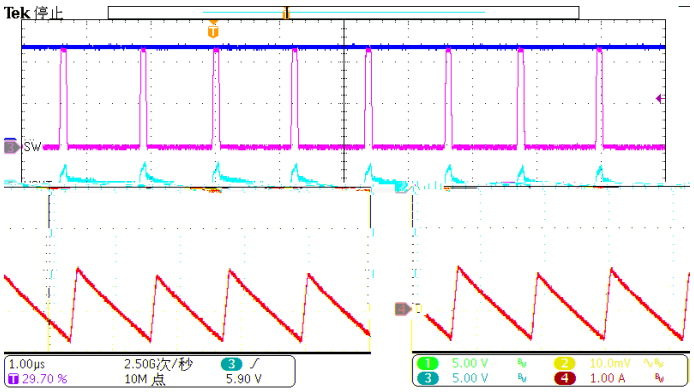

Tek 预览
Vin
PG
VOUT
IL
5.00 V
1.00 V
5.00 A
10.0ms
29.70 %
100M次/秒
10M 点
500mV

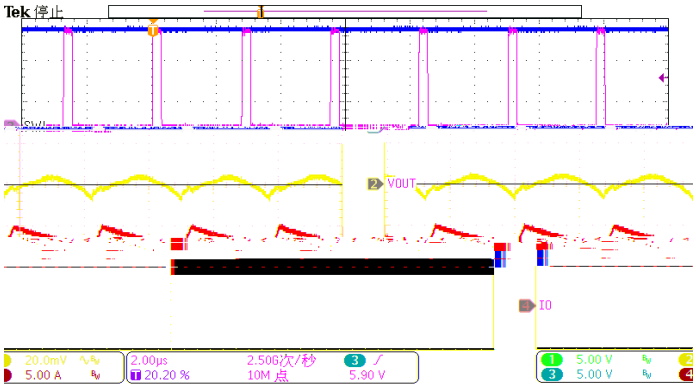

Tek 停止
Vin
PG
VOUT
IL
5.00 V
1.00 V
10.0ms
100M次/秒

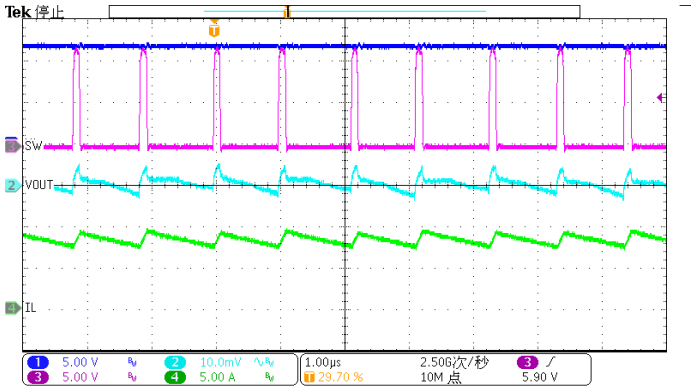

Tek 停止
VIN
PG
VOUT
IL
5.00 V
5.00 V
1.00 V
5.00 A
10.0ms
30.10 %
100M次/秒
10M 点
500mV

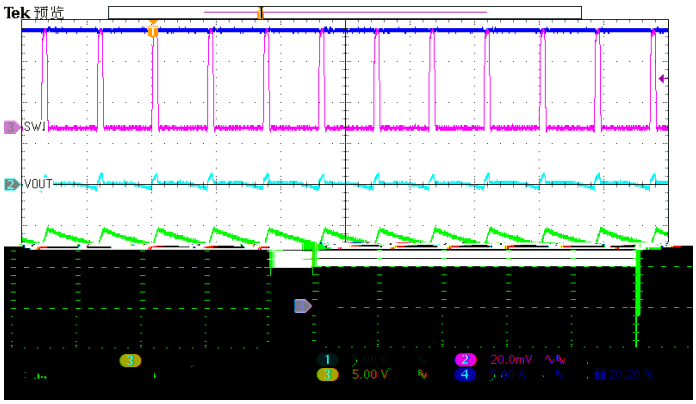

Tek 停止
VIN
PG
VOUT
1.00 V
5.00 A
30.10 %
5.00 V
5.00 V

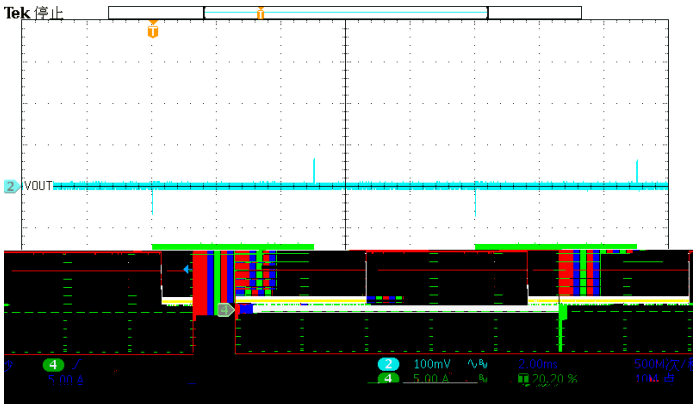

Tek 预览
SW
VOUT
5.00 V
5.00 V
10.0mV
1.00 A
10.0µs
29.70 %
2.50G次/秒
10M 点
5.90 V

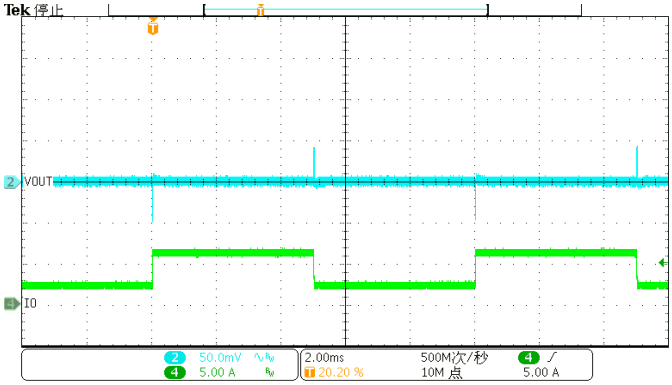

Tek 停止
SW
1.00µs
29.70 %
2.50G次/秒
10M 点
5.90 V
5.00 V
5.00 V
10.0mV
1.00 A

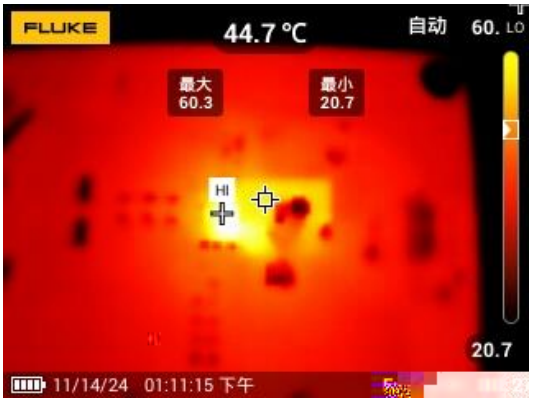

Tek 停止
VOUT
IO
20.0mV
5.00 A
2.00µs
20.20 %
2.50G次/秒
10M 点
5.90 V
5.00 V
5.00 V


Tek 停止
SW
VOUT
IL
5.00 V
5.00 V
10.0mV
5.00 A
1.00µs
29.70 %
2.50G次/秒
10M 点
5.90 V


Tek 预览
SW1
VOUT
20.0mV
5.00 V
20.20 %


Tek 停止
VOUT
100mV
2.00ms
5.00 A
20.20 %


Tek 停止
VOUT
IO
50.0mV
5.00 A
2.00ms
20.20 %
500M次/秒
10M 点
5.00 A


FLUKE
44.7 °C
自动
60. LO
最大
60.3
最小
20.7
HI
20.7
11/14/24 01:11:15 下午

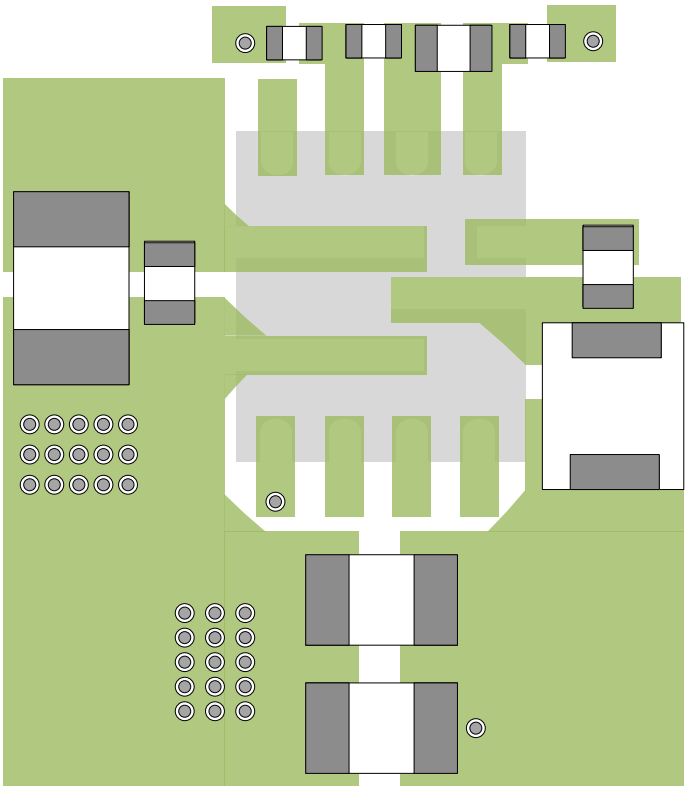
1.
2.

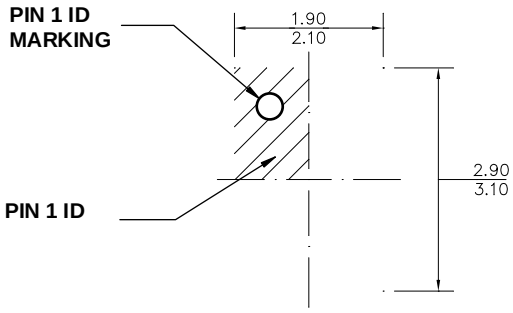
3.

4.

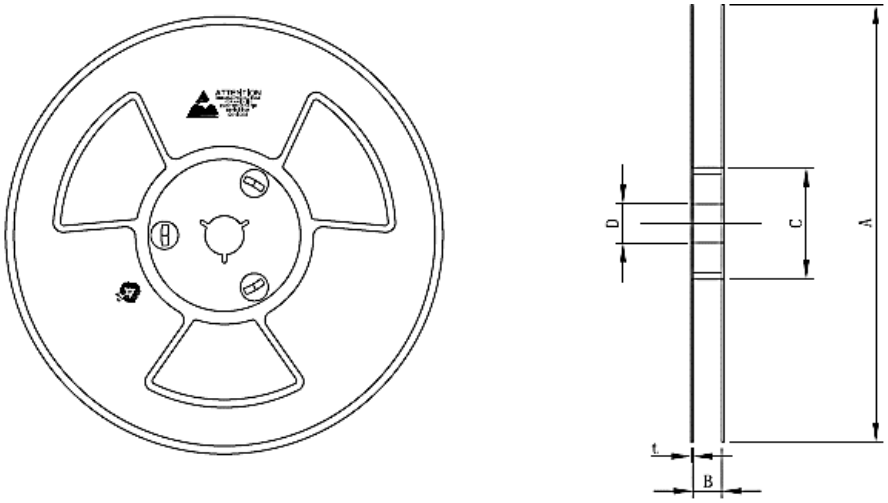
5.

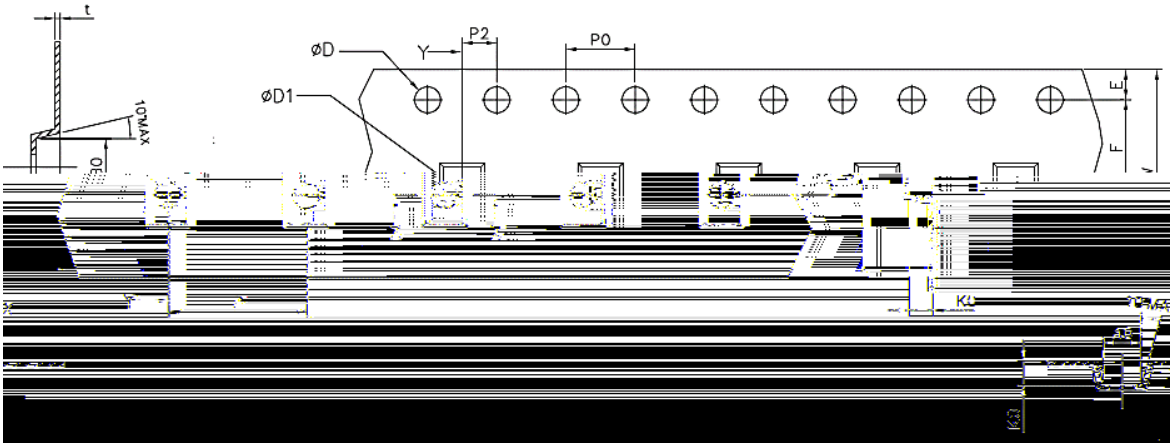
6.





1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.


D
C
A
t
B


t
ØD
Y
P2
P0
ØD1
E
F
K0