3.8V-32V Vin, 1.1MHz, 2A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 3.3V ±1% Output Voltage (SCT2323)
- 5V ±1% Output Voltage (SCT2325)
- Fully Integrated 130 R_{dson} High-side MOSFET and 70 R_{dson} Low-side MOSFET
- 1uA Shut-down Current
- 20uA Ultra Low Quiescent Current
- 1.1MHz Switching Frequency with ±6% Frequency Spread Spectrum FSS Modulation
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Drop-Out LDO Operation
- Pulse Skipping Modulation PSM in Light Load
- 4ms Built-in Soft-start Time
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

APPLICATIONS

- White Goods, Air Conditioner, Refrigerator etc.
- Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer
- DTV, STB, Monitor/LCD Display
- E-meter

DESCRIPTION

The SCT2323 and SCT2325 are 2A, 1.1MHz, synchronous buck converters with up to 32V wide input voltage range, which fully integrates a 130 high-side MOSFET and

The SCT232

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.1: Released for Production. Complete orderable part number

Revision 1.2: Delete FB in ABS table

Revision 1.3: Update Device Order Information

DEVICE ORDER INFORMATION

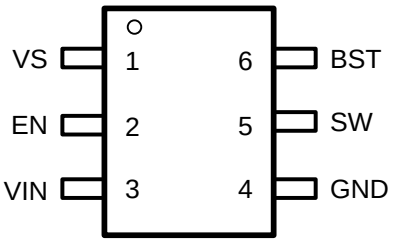
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2323TVBR	Tape & Reel	3000	2323	6	TSOT23-6L
SCT2325TVBR	Tape & Reel	3000	2325	6	TSOT23-6L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
VS	-0.3	6	V
Operating junction temperature(2)	-40	125	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: TSOT23-6L, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VS	1	Buck converter output Pin. SCT2323 output voltage is 3.3V and SCT2325 output voltage is fixed as 5V
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply so as to be connected VIN directly to enable the device. The device has precision enable threshold 1.18V/1,1V rise/fall for programmable UVLO threshold and hysteresis.
VIN	3	Power supply input. Must be locally bypassed.
GND	4	Power ground. Must be soldered directly to ground planes.
SW	5	Switching node of the buck converter.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	32	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6L	UNIT
R	Junction to ambient thermal resistance		

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		32	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		3.5	3.7	V
	Hysteresis			420		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	3	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V.		20		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.18	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN}	Enable pin input current	EN=1V	1	1.5	2	uA
I_{EN_HYS}	Enable pin hysteresis current	EN=1.5V		4		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			130		
R_{DSON_L}	Low side FET on-resistance			70		
Output Voltage						
V_S	Output Voltage(SCT2323)		3.267	3.3	3.333	V
	Output Voltage(SCT2325)		4.95	5	5.05	V
Current Limit						
I_{LIM_HSD}	HSD peak current limit		2.5	2.8	3.1	A
I_{LIM_HSD}	LSD valley current limit		2.8	3.2	3.6	
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V	0.99	1.1	1.21	MHz
t_{ON_MIN}	Minimum on-time			80		ns
F_{JITTER}	FSS percentage			±6		%
Soft Start Time						
t_{SS}	Internal soft-start time			4		ms
Protection						
V_{OVP}	Output overvoltage protection threshold	V_{OUT} rising		110		%
	Hysteresis			5		%
T_{HIC_W}	Over current protection hiccup wait time			512		Cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		Cycles
T_{SD}	Thermal shutdown threshold	T_J rising		160		°C
	Hysteresis	T_J falling below TSD		25		°C

TYPICAL CHARACTERISTICS

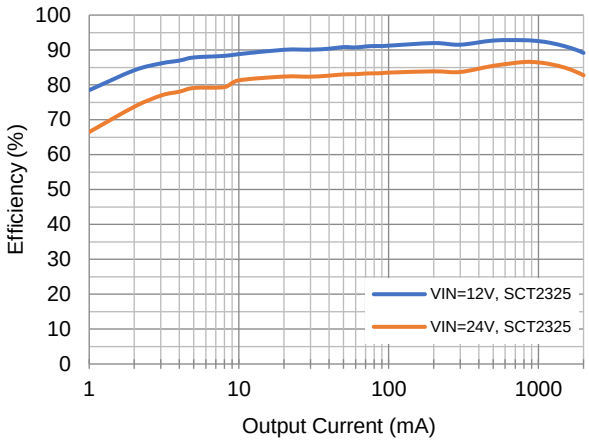


Figure 1. SCT2325 Efficiency, Vout=5V

Figure 2. SCT2323 Efficiency, Vout=3.3V

Figure 3. Shut down Current vs Temperature

Figure 4. Quiescent Current vs Temperature

Figure 5. Output Voltage & Temperature

Figure 6. Peak Current Limit & Temperature

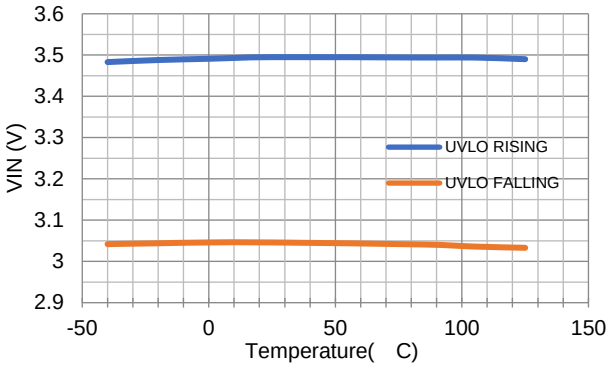


Figure 7. VIN UVLO & Temperature

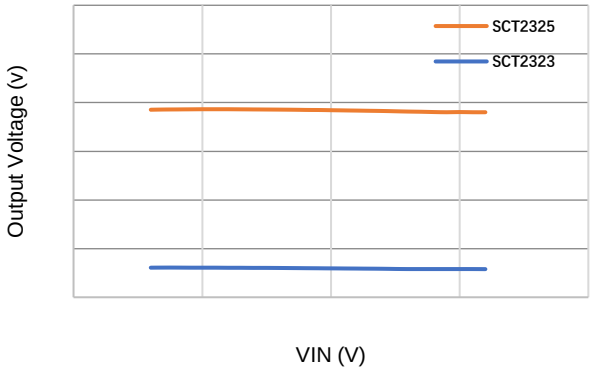


Figure 8. Line Regulation (SCT2323, SCT2325), ILoad=2A

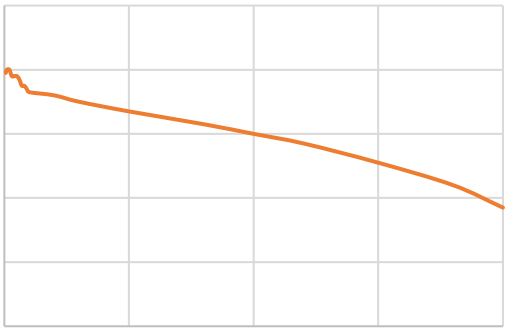
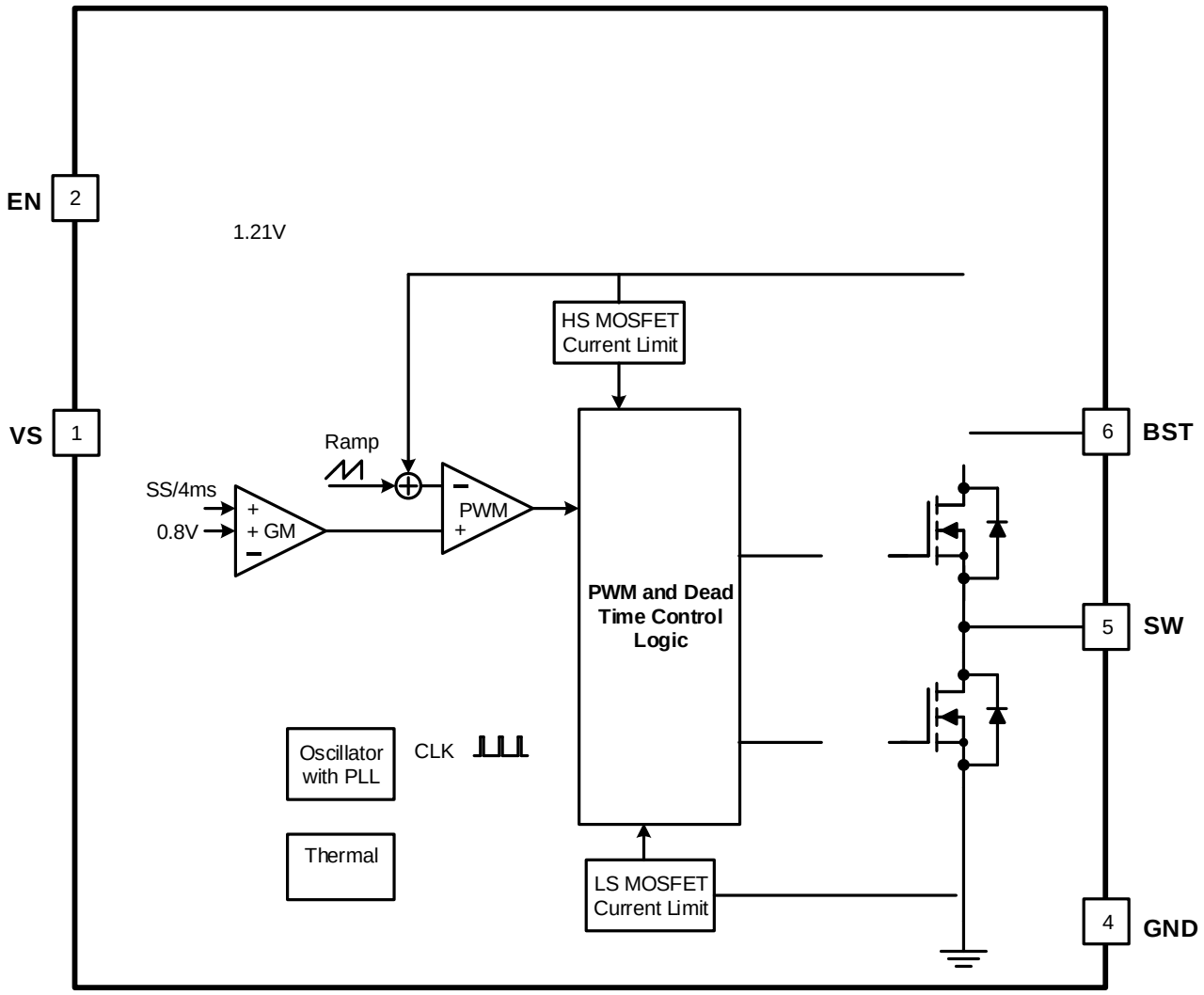


Figure 9. Load Regulation, Vout=5V

Figure 10. Load Regulation, Vout=3.3V

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT2323 and SCT2325 devices are 3.8V-32V input converters. The device employs fixed frequency peak cu initiates turning on the integrated high-side power MOS and the converter charges output cap. When sensed vo voltage of internal COMP (see functional block diagram low-side MOSFET Q2. The inductor current decreases cycle, the low-side MOSFET Q2 turns off. This repeats

The peak current mode control with the internal loop co the SCT2323 and SCT2325 footprints and minimize the integrate the output voltage feedback resistor divider n The SCT2323 has the 3.3V output and the SCT2325 ha

The error amplifier serves the COMP node by compari with an internal 0.8V reference voltage. When the loa relative to the reference raises COMP voltage till the av This feedback loop well regulates the output voltage. T circuitry to prevent sub-harmonic oscillation when duty c mode control.

The quiescent current of SCT2323 or SCT2325 is 20u disabling the device, the supply shut down current is onl Mode (PSM) to further increase the power efficiency i achieved up to 88% at 5mA load condition.

The SCT2323 and SCT2325 implement the Frequenc centered 1.1MHz switching frequency. FSS improves E any one receiver band for a significant length of time. T switching node voltage ringing-free without sacrificin frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during pr wait time is 512 cycles and the hiccup restart time is 819 full protections including cycle high current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2323 and SCT2325 are designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2323 and SCT2325 feature Under Voltage Lock Out(UVLO) functions. The default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V rising), the SCT2323 and SCT2325 enable all functions and the devices start soft-start phase. The SCT2323 and SCT2325 have the built-in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V falling).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 11. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin, and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

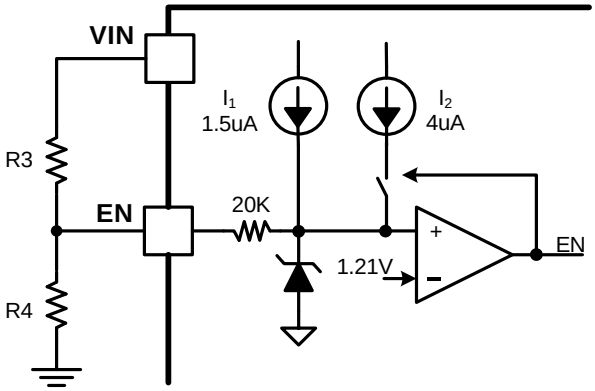


Figure 11. Adjustable VIN UVLO

(1)

(2)

Where,
Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=4uA
V_{ENR}=1.18V
V_{EMF}=1.1V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

In some applications, the system EMI test must meet EMI standards EN55011 and EN55022. To improve EMI performance, the SCT2323 and SCT2325 adopt Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at a particular frequency. The SCT2323 and SCT2325 feature 1.1MHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 1.1MHz to a range 1034KHz ~ 1166KHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2323 and SCT2325 implement the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Proprietary Design). The switching node zoomed in wave form is shown in Figure 12.

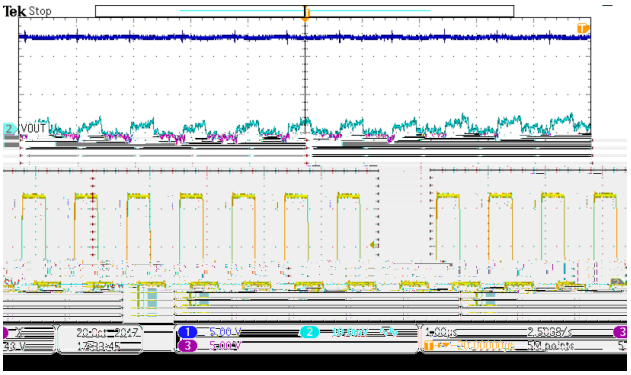


Figure 12. Switching Node Waveform

Peak Current Limit and Hiccup Mode

The SCT2323 and SCT2325 have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during over current condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

The SCT2323 and SCT2325 feature the output over-voltage protection (OVP). If the output pin voltage exceeds 110% of reference output voltage (5V or 3.3V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of set output voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

Pulse Skipping Modulation PSM Mode

In heavy load condition, the SCT2323 and SCT2325 force the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 450mA peak inductor current. When the load current approaches zero, the SCT2323 and SCT2325 enter Pulse Skipping Modulation (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1

forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2323 and SCT2325 intervene to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-Out LDO Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop-Out (LDO) operation is implemented by the SCT2323 or SCT2325. The Low Drop Out operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation

In LDO operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 13.

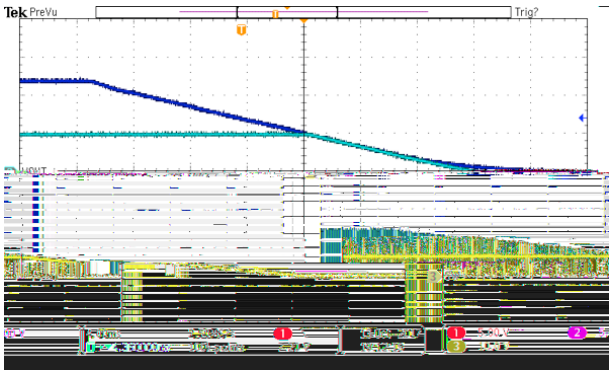


Figure 13. LDO Operation During Power Down

Thermal Shutdown

Once the junction temperature in the SCT2323 or SCT2325 exceeds 160C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

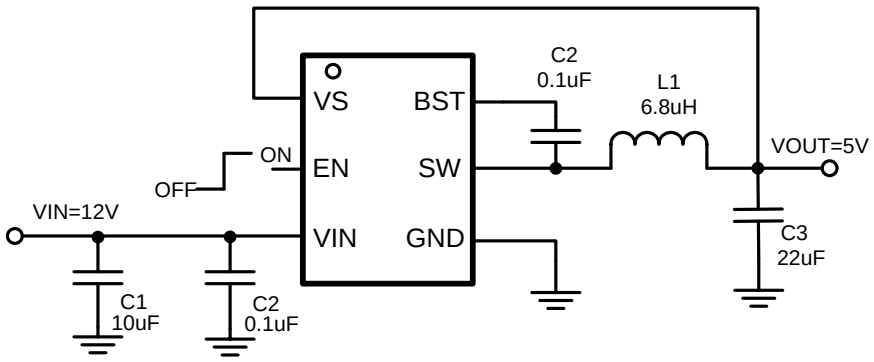


Figure 14. 12V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	

have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2323 and SCT2325. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744314101 is used on SCT2323 and SCT2325 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744314101	10	33	3.5	7x7x5	Wurth Electronik

- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

Output Feed-Forward Capacitor Selection

The SCT2323 and SCT2325 have the internal integrated loop compensation as shown in the function block diagram. Thetsin theTm2 0 612 792 reW* n0al integrated loop 85.58 378.07 32.52 reW*39(dn2* nBT/F16 6.94b)-9Qq9.* nBr

Application Waveforms

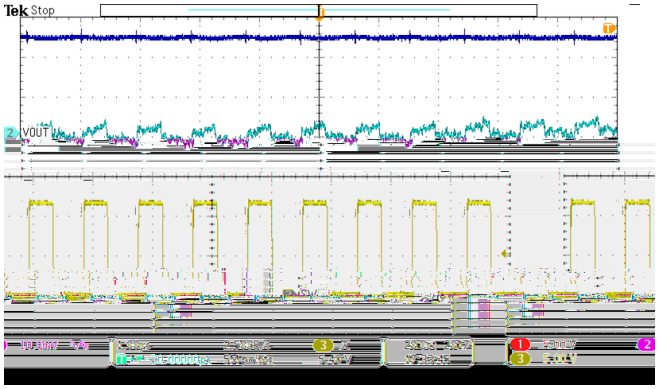


Figure 15. SW node waveform and Output Ripple, Iout=2A

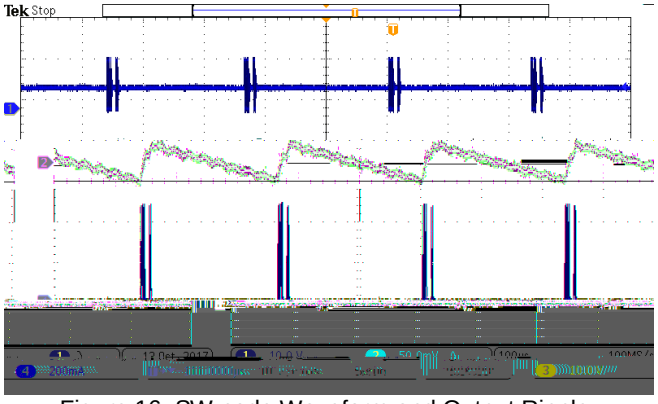


Figure 16. SW node Waveform and Output Ripple, Iout=10mA

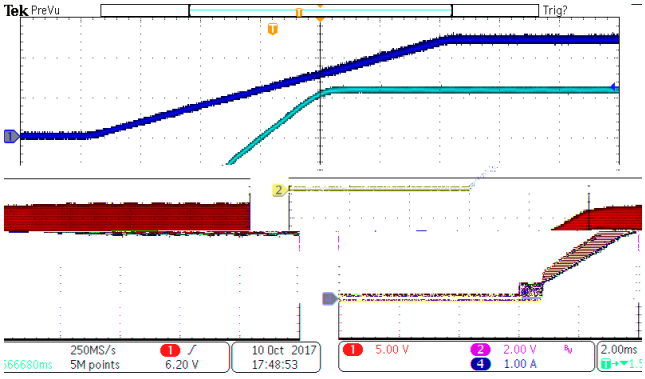


Figure 17. Power Up, Iout=2A

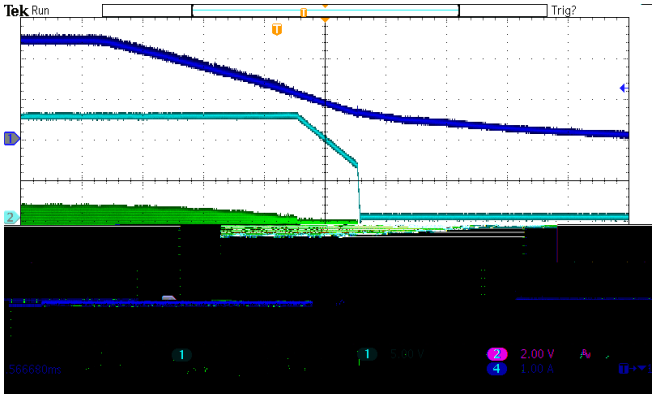


Figure 18. Power Down, Iout=2A

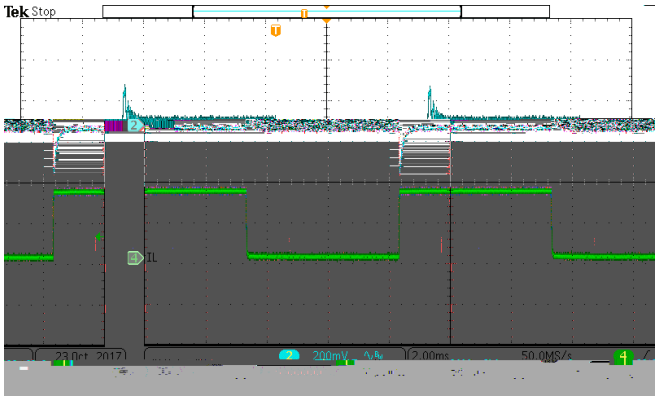


Figure 19. Load Transient
(Vout=5V, Iout=0.2A to 1.8A,SR=250mA/us)

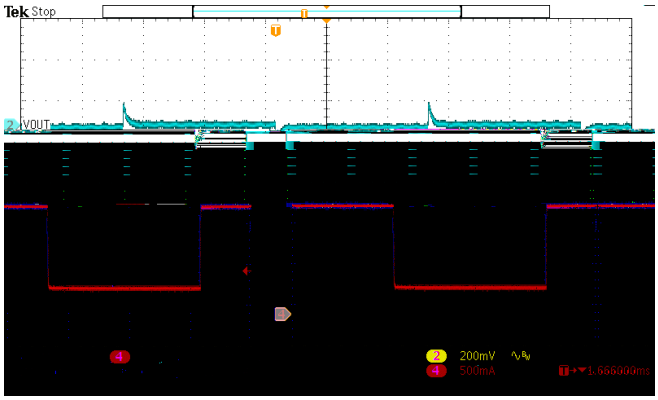


Figure 20. Load Transient
(Vout=5V, Iout=0.5A to 1.5A,SR=250mA/us)

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21 is the recommended PCB layout of the SCT2323 and SCT2325.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

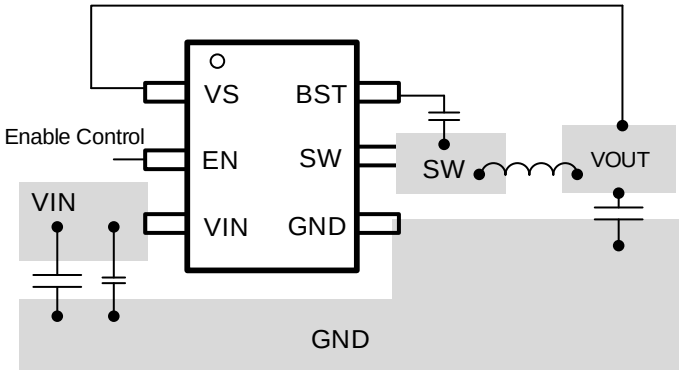
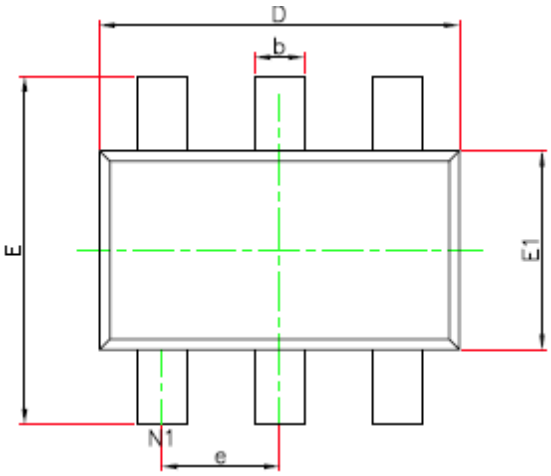


Figure 21. PCB Layout Example

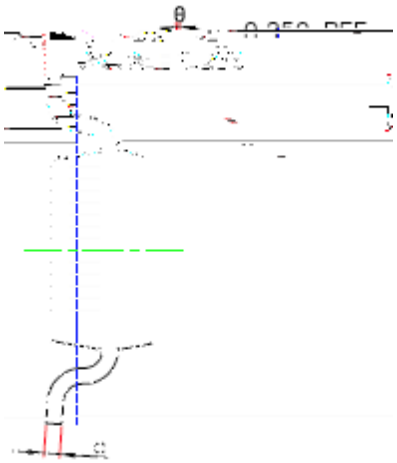
Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$.

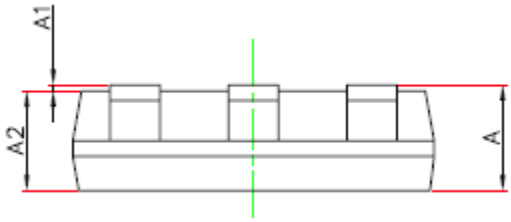
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



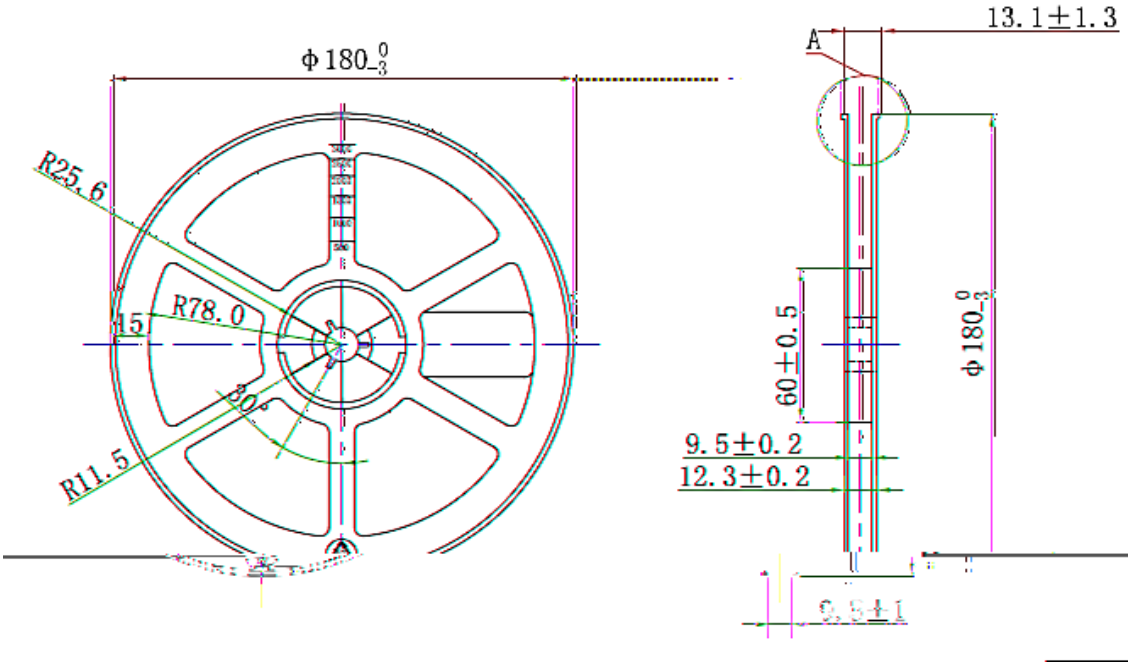
SIDE VIEW

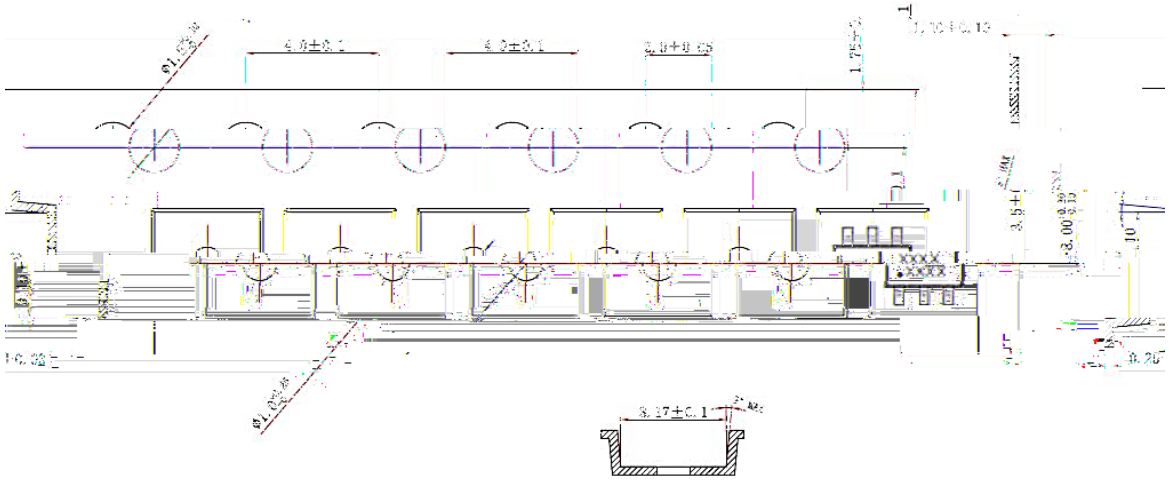
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-------		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
	0		8

TAPE AND REEL INFORMATION





Feeding Direction

RELATED PARTS

PART NUMBERS	DESCRIPTION	COMMENTS
SCT2320 **SCT2330**	3.8V-32V Vin, 2A/3A, 500kHz Synchronous Buck Converter with EMI Reduction	• 20uA quiescent current • 500kHz switching frequency with ±6% frequency spread spectrum. • EMI reduction with switching node ringing-free.
SCT2321 **SCT2331**	3.8V-32V Vin, 2A/3A, 500kHz Synchronous Buck Converter with PWM Mode	• Forced PWM mode operation. • Fixed 500kHz Switching Frequency.

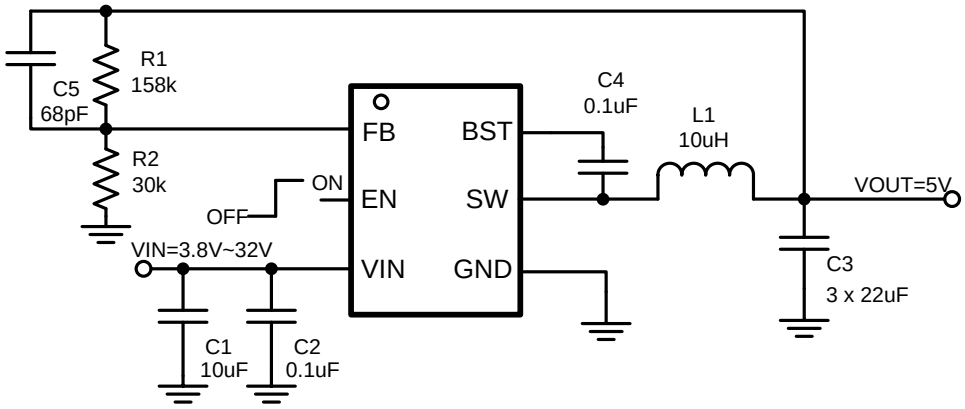


Figure 22. SCT2320 and SCT2321 Typical Application

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